



SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution



Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A+' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB302–VLSI DESIGN

III YEAR/ V SEMESTER

UNIT 1 –MOS TRANSISTOR PRINCIPLE

TOPIC 8 –CMOS INVERETER DC CHARACTERISTICS



OUTLINE



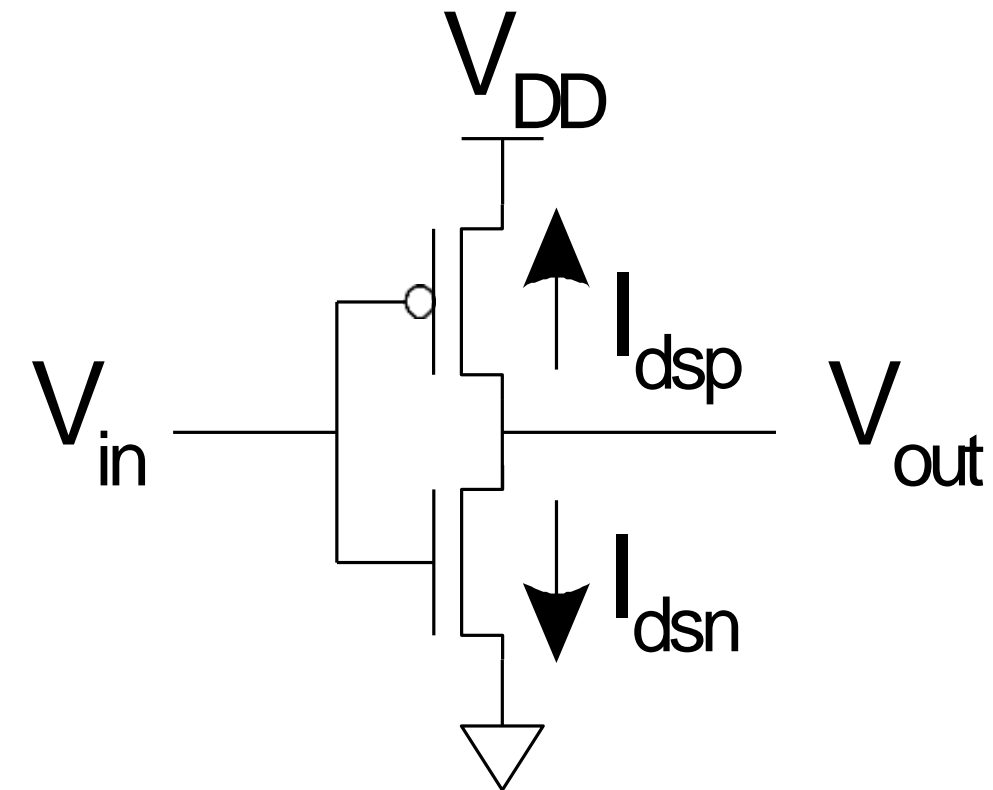
- INTRODUCTION
- DC RESPONSE
- LOGIC LEVELS AND NOISE MARGINS
- ACTIVITY
- TRANSIENT RESPONSE
- ASSESSMENT
- SUMMARY



DC RESPONSE



- DC Response: V_{out} vs. V_{in} for a gate
- Ex: Inverter
 - When $V_{in} = 0 \rightarrow V_{out} = V_{DD}$
 - When $V_{in} = V_{DD} \rightarrow V_{out} = 0$
 - In between, V_{out} depends on transistor size and current
 - By KCL, must settle such that
$$I_{dsn} = |I_{dsp}|$$
 - We could solve equations
 - But graphical solution gives more insight





TRANSISTOR OPERATION



- Current depends on region of transistor behavior
- For what V_{in} and V_{out} are nMOS and pMOS in
 - Cutoff?
 - Linear?
 - Saturation?



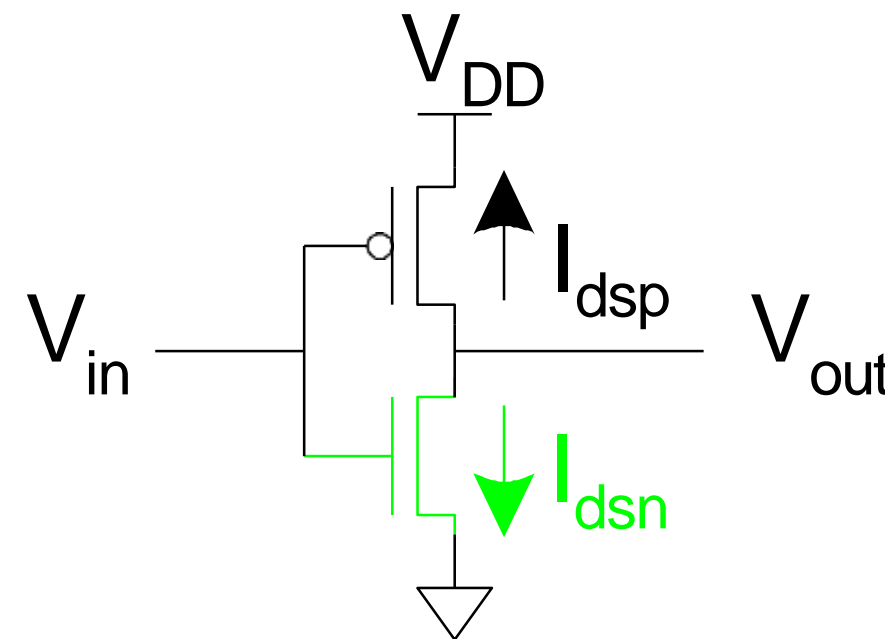
NMOS OPERATION



Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$ $V_{in} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$ $V_{out} < V_{in} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$ $V_{out} > V_{in} - V_{tn}$

$$V_{gsn} = V_{in}$$

$$V_{dsn} = V_{out}$$





PMOS OPERATION

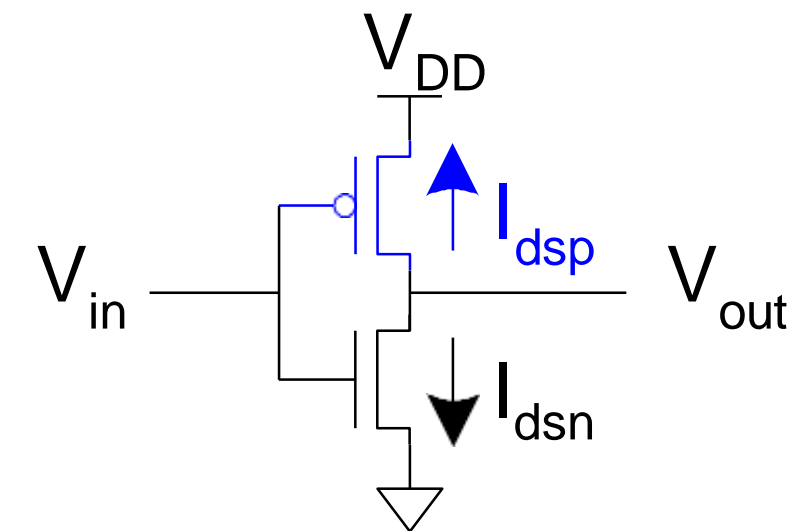


Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$ $V_{in} > V_{DD} + V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$

$$V_{gsp} = V_{in} - V_{DD}$$

$$V_{dsp} = V_{out} - V_{DD}$$

$$V_{tp} < 0$$

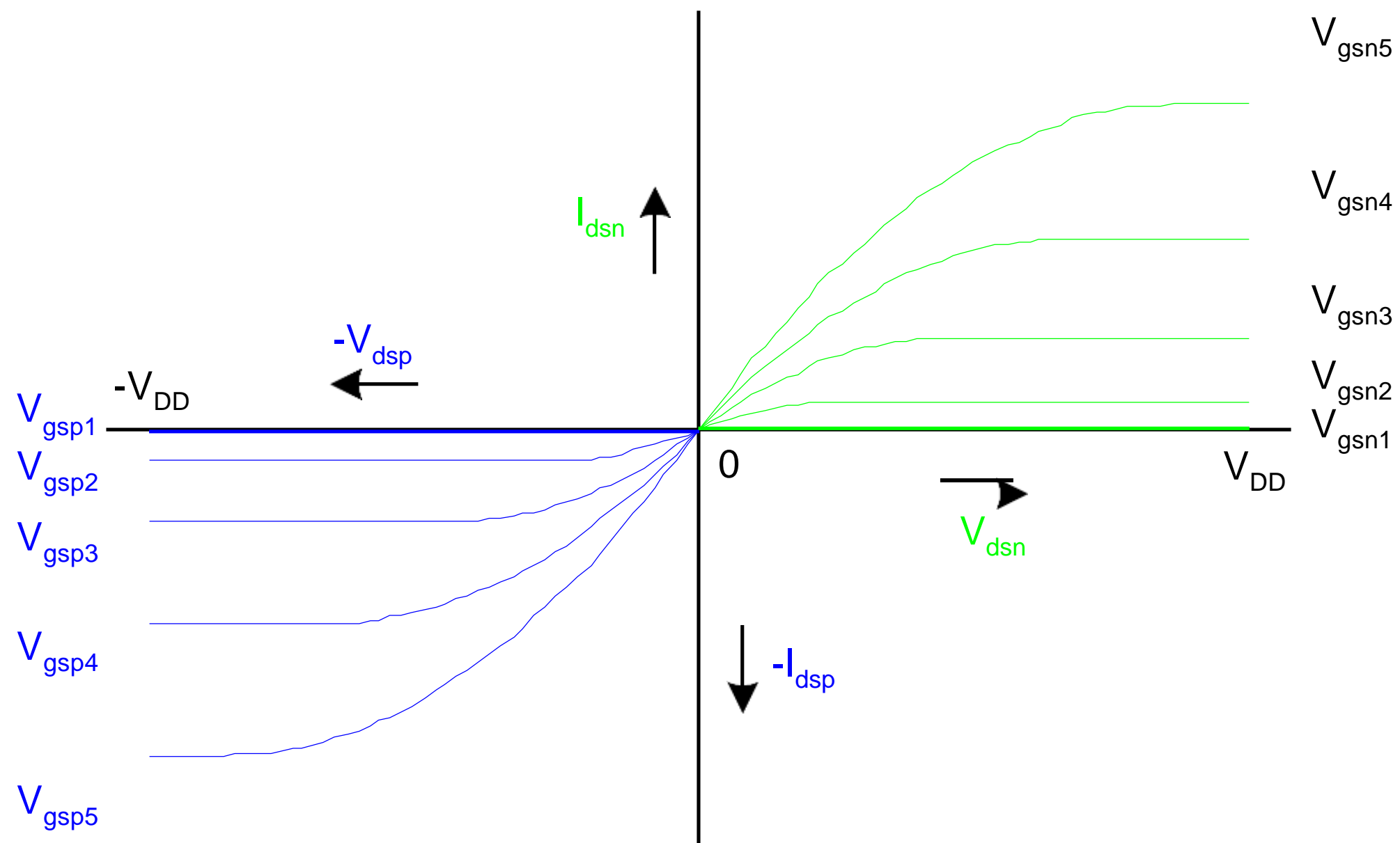




I-V CHARACTERISTICS

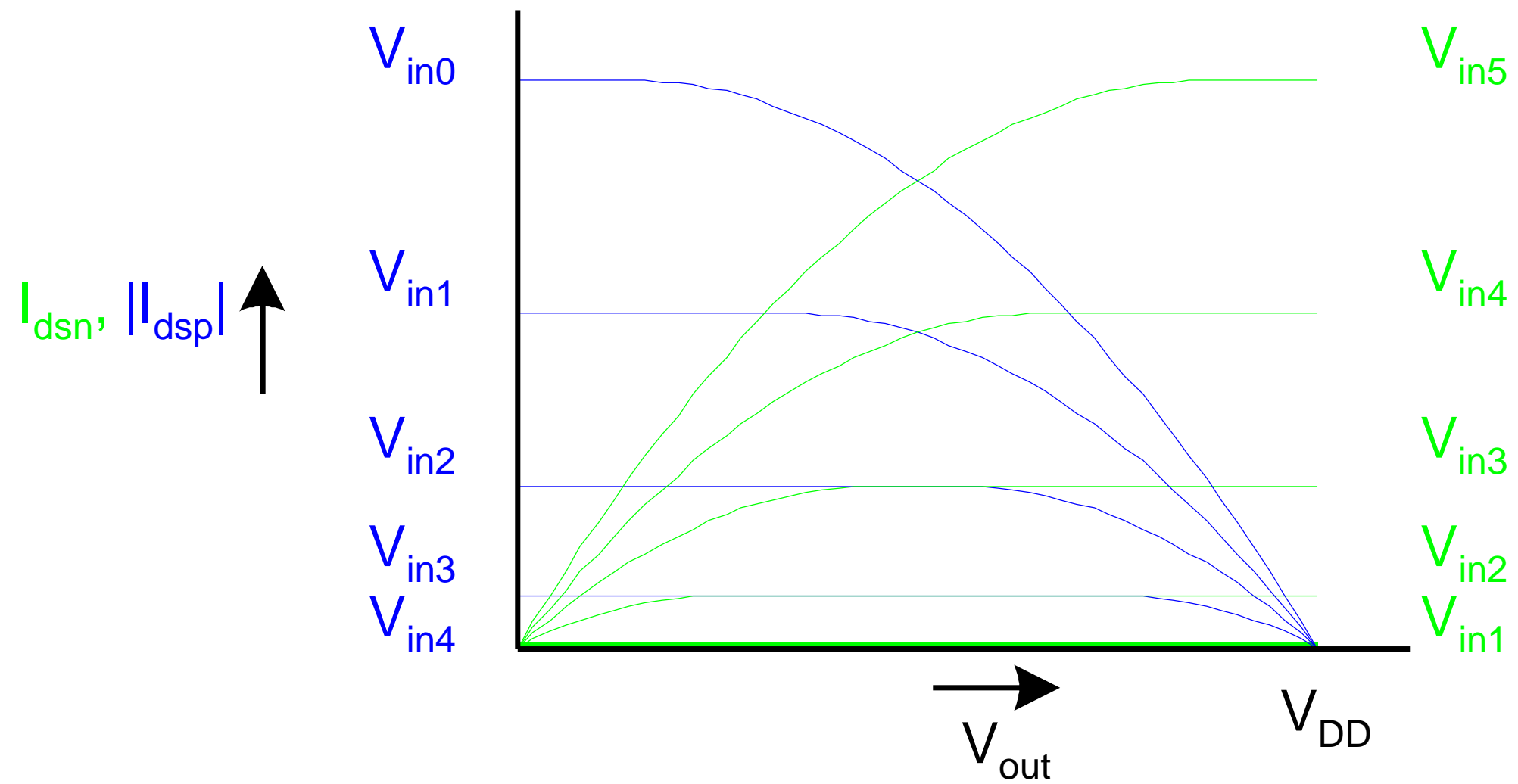


Make pMOS is wider than nMOS such that $\beta_n = \beta_p$





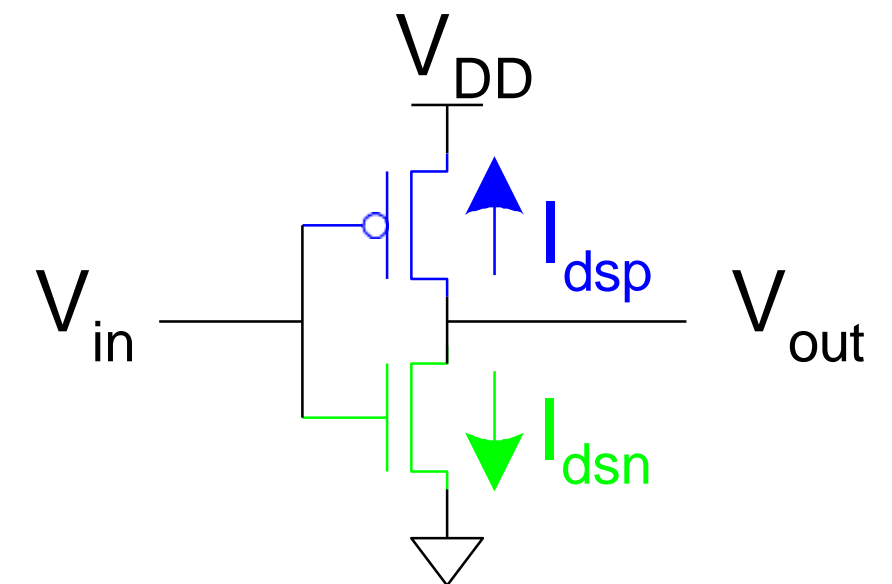
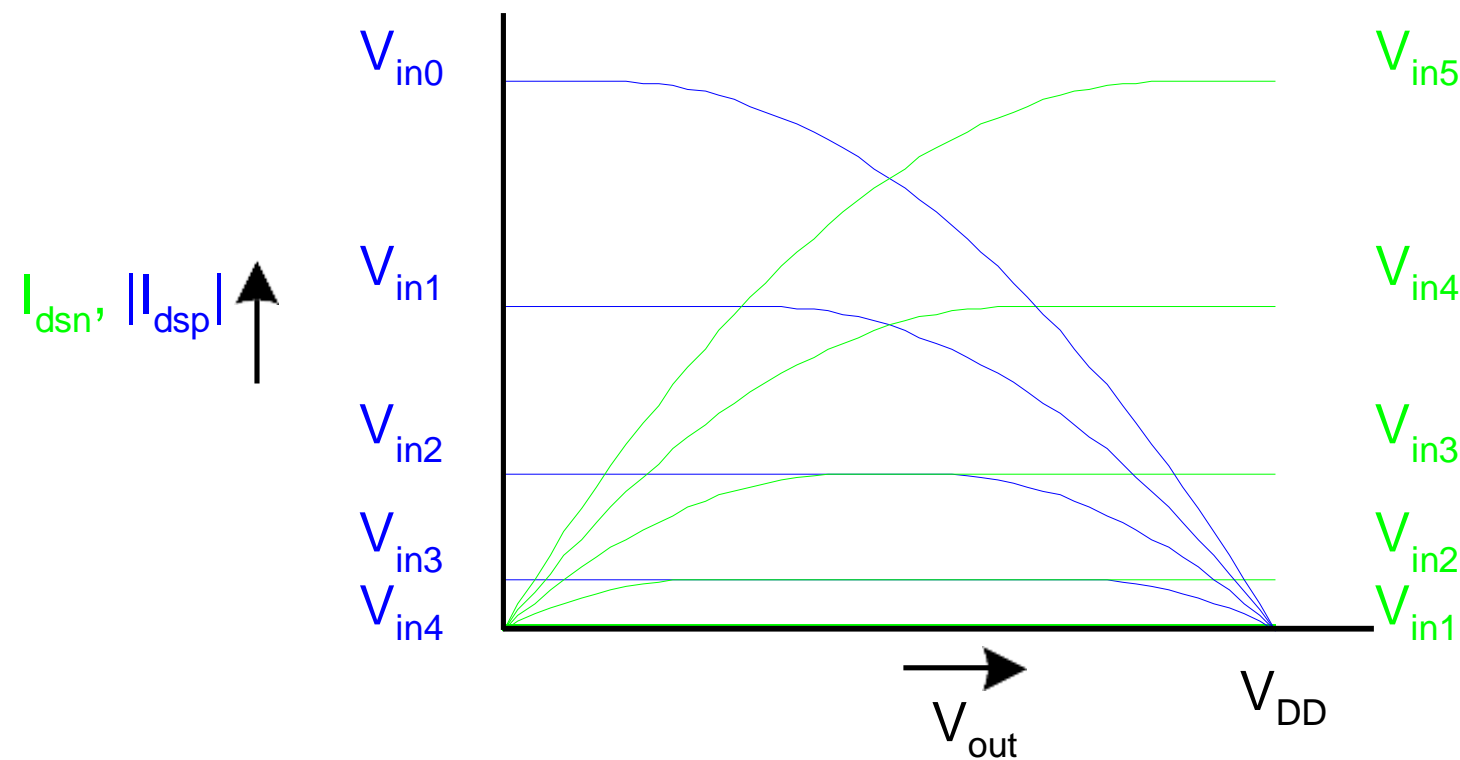
CURRENT VS V_{OUT} , V_{IN}





LOAD LINE ANALYSIS

- For a given V_{in} :
 - Plot I_{dsn} , I_{dsp} vs. V_{out}
 - V_{out} must be where |currents| are equal in



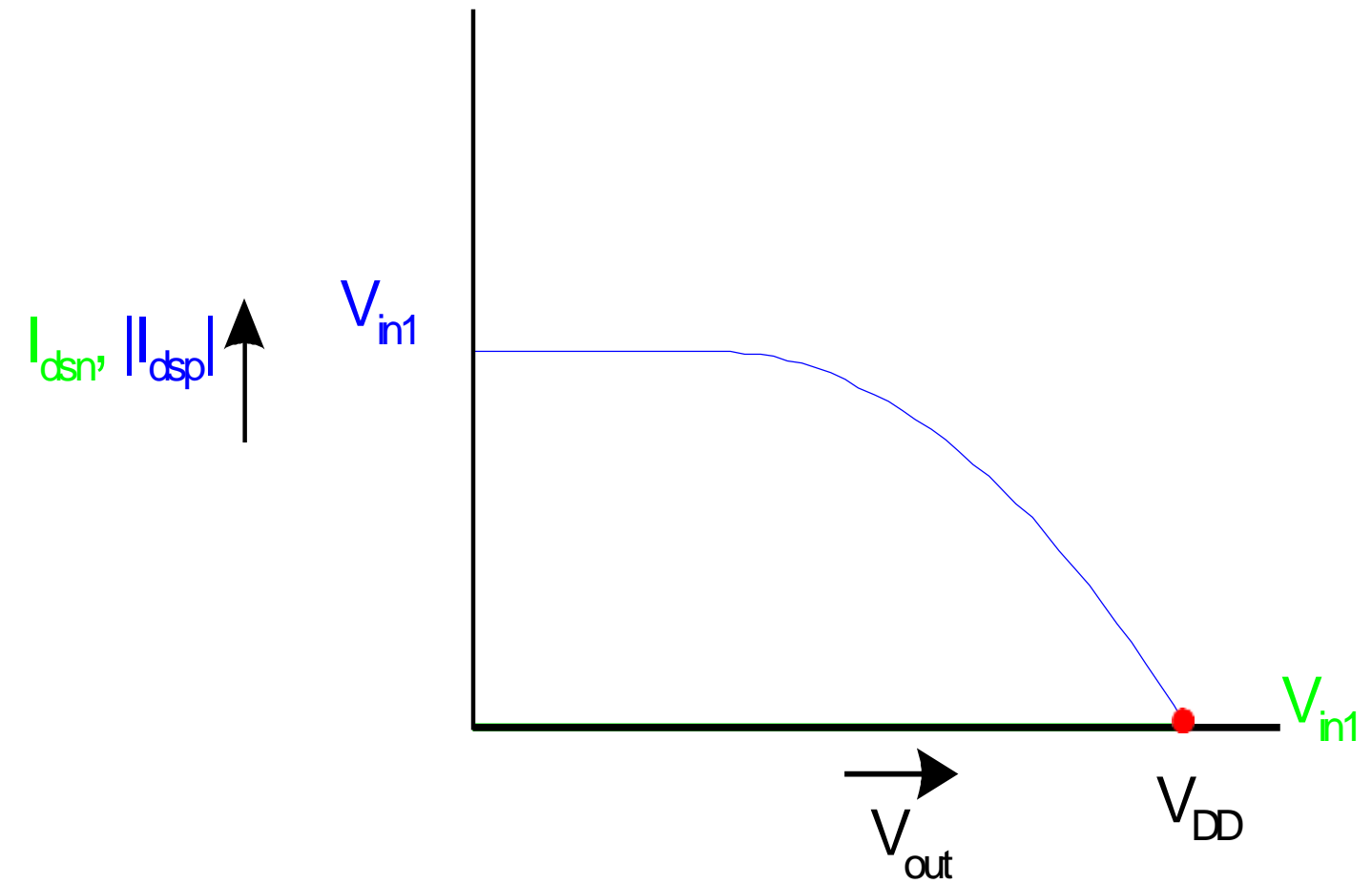
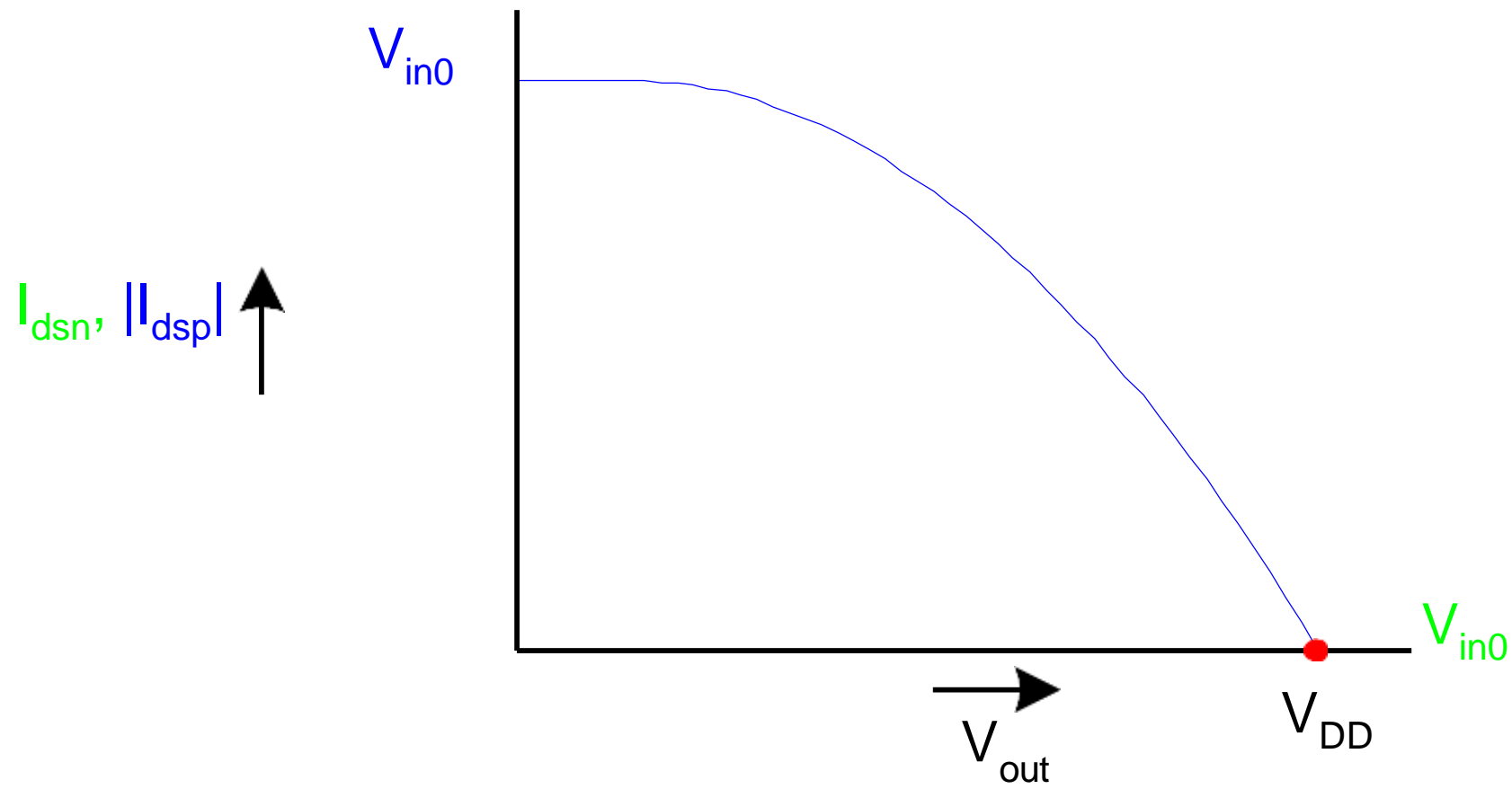


LOAD LINE ANALYSIS



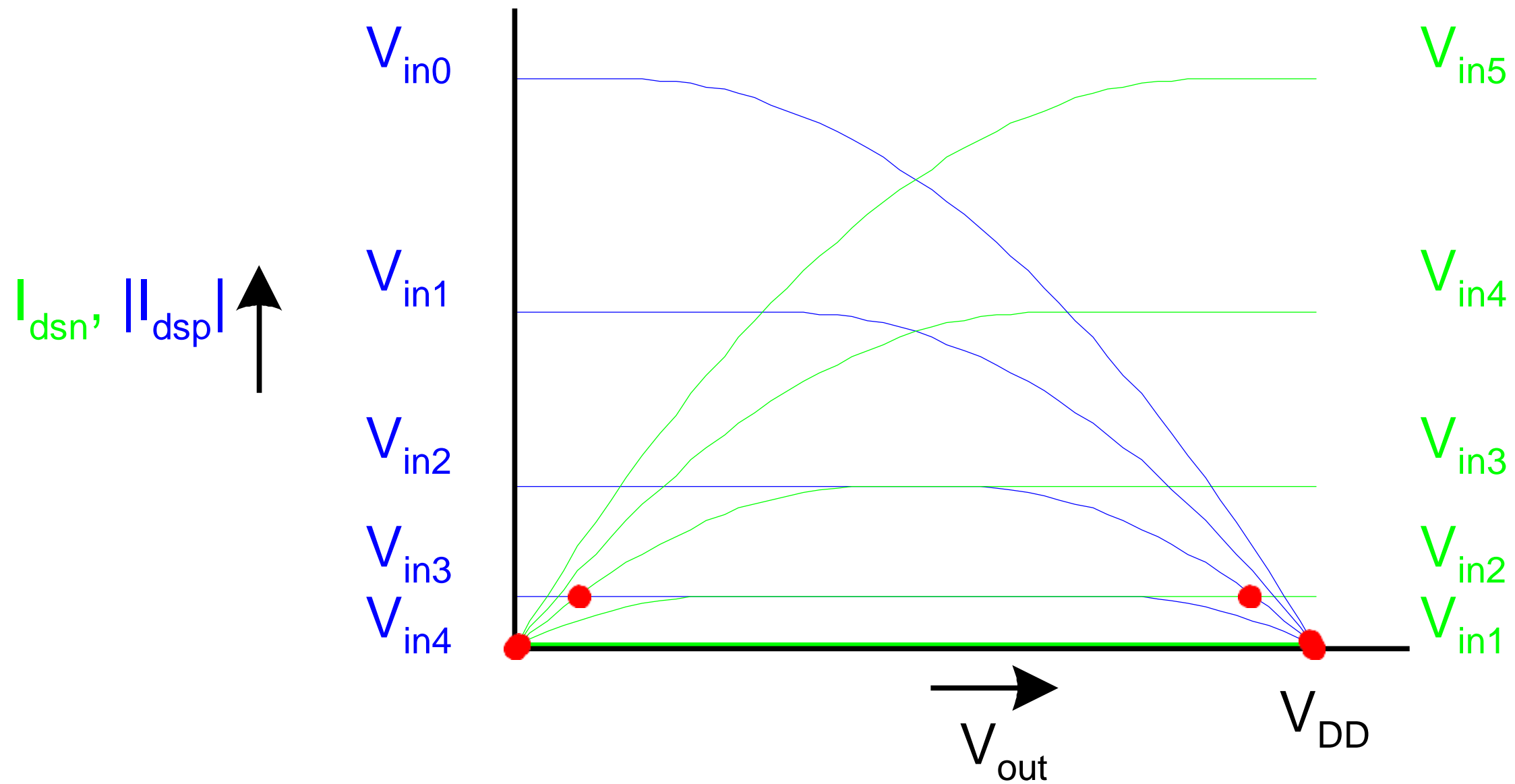
$$V_{in} = 0$$

$$V_{in} = 0.2V_{DD}$$





LOAD LINE ANALYSIS SUMMARY

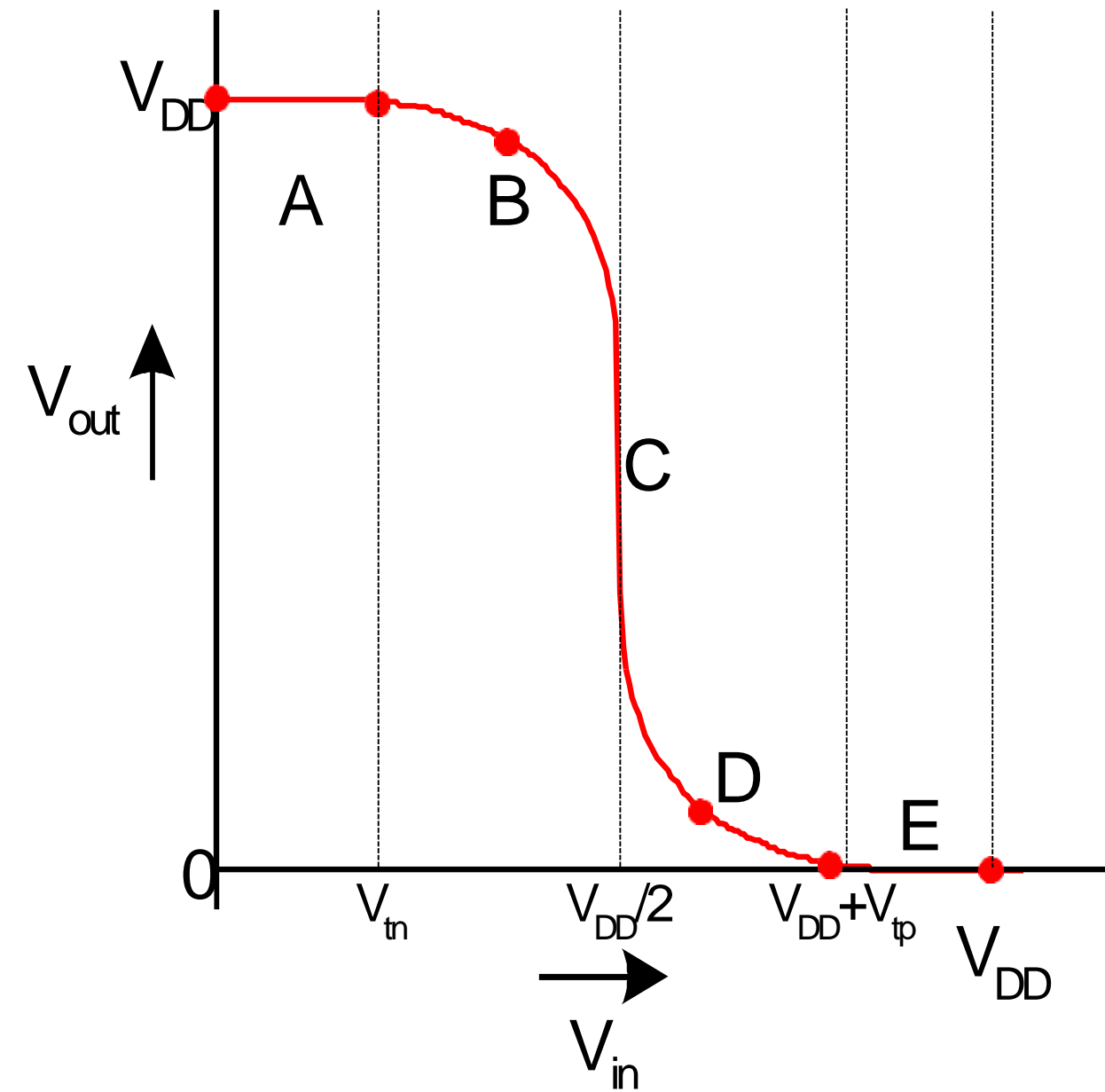
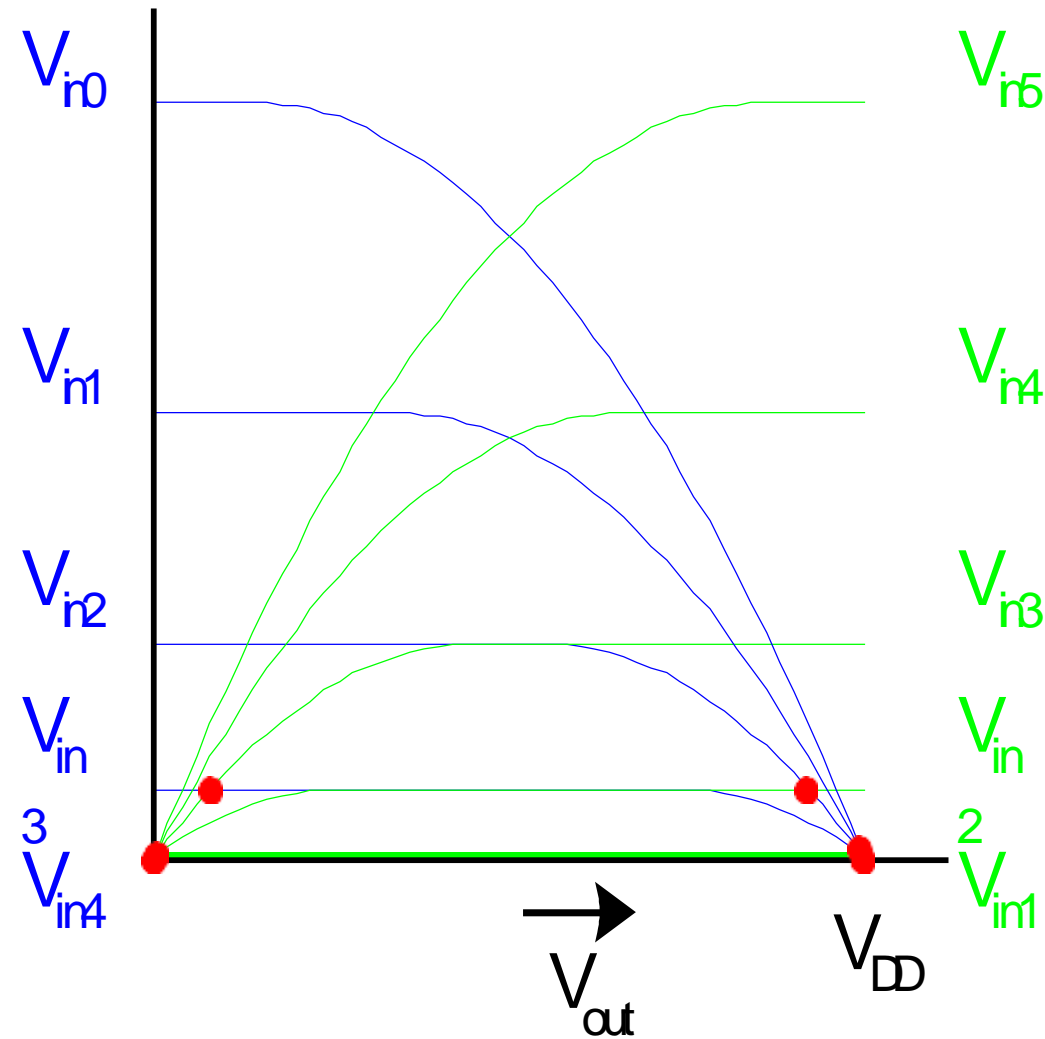




DC TRANSFER CURVE



Transcribe points onto V_{in} vs. V_{out} plot

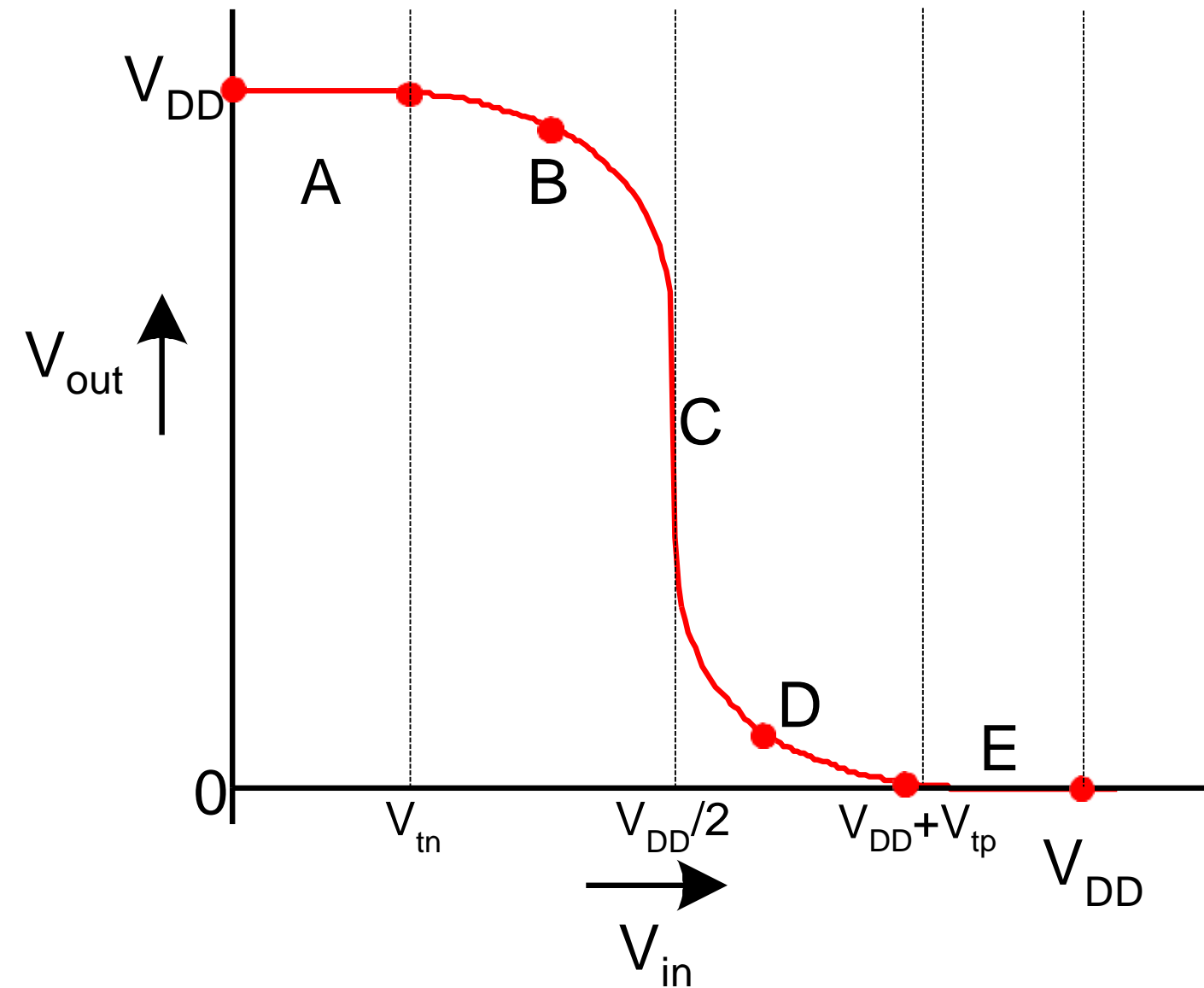




REVISIT TRANSISTOR OPERATING REGIONS



Region	nMOS	pMOS
A	Cutoff	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cutoff

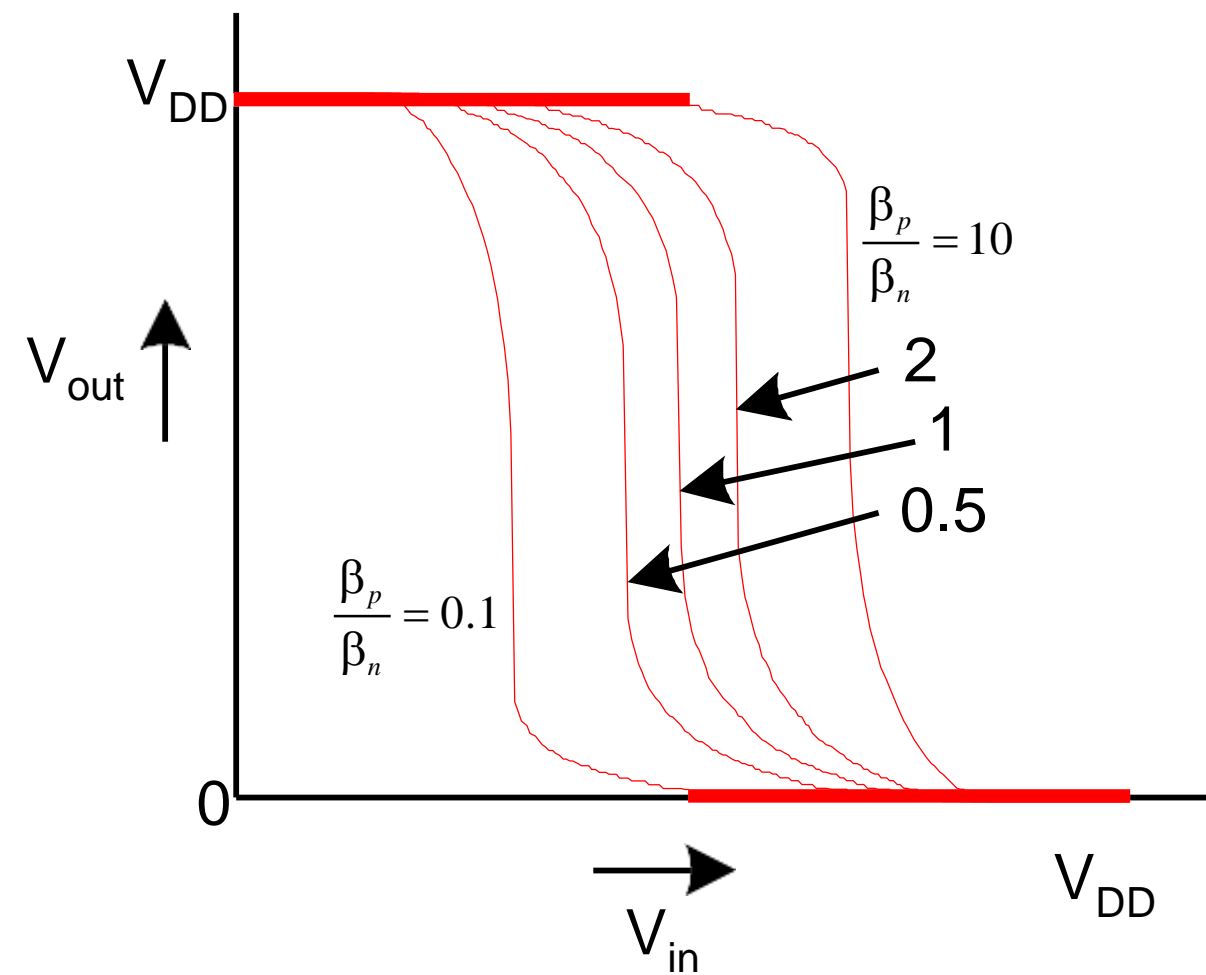




BETA RATIO



If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$ Called skewed gate
Other gates: collapse into equivalent inverter

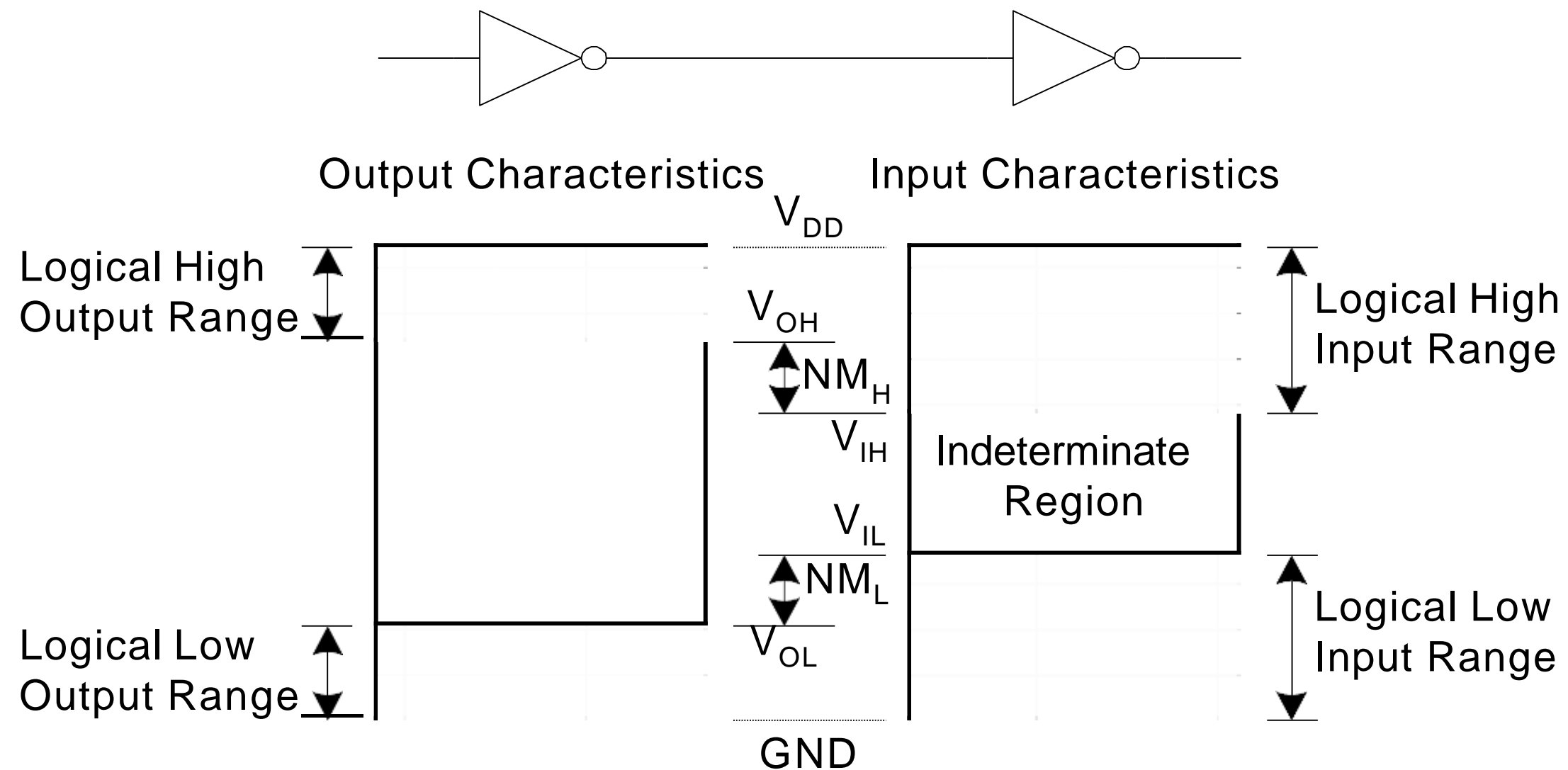




NOISE MARGINS



How much noise can a gate input see before it does not recognize the input?

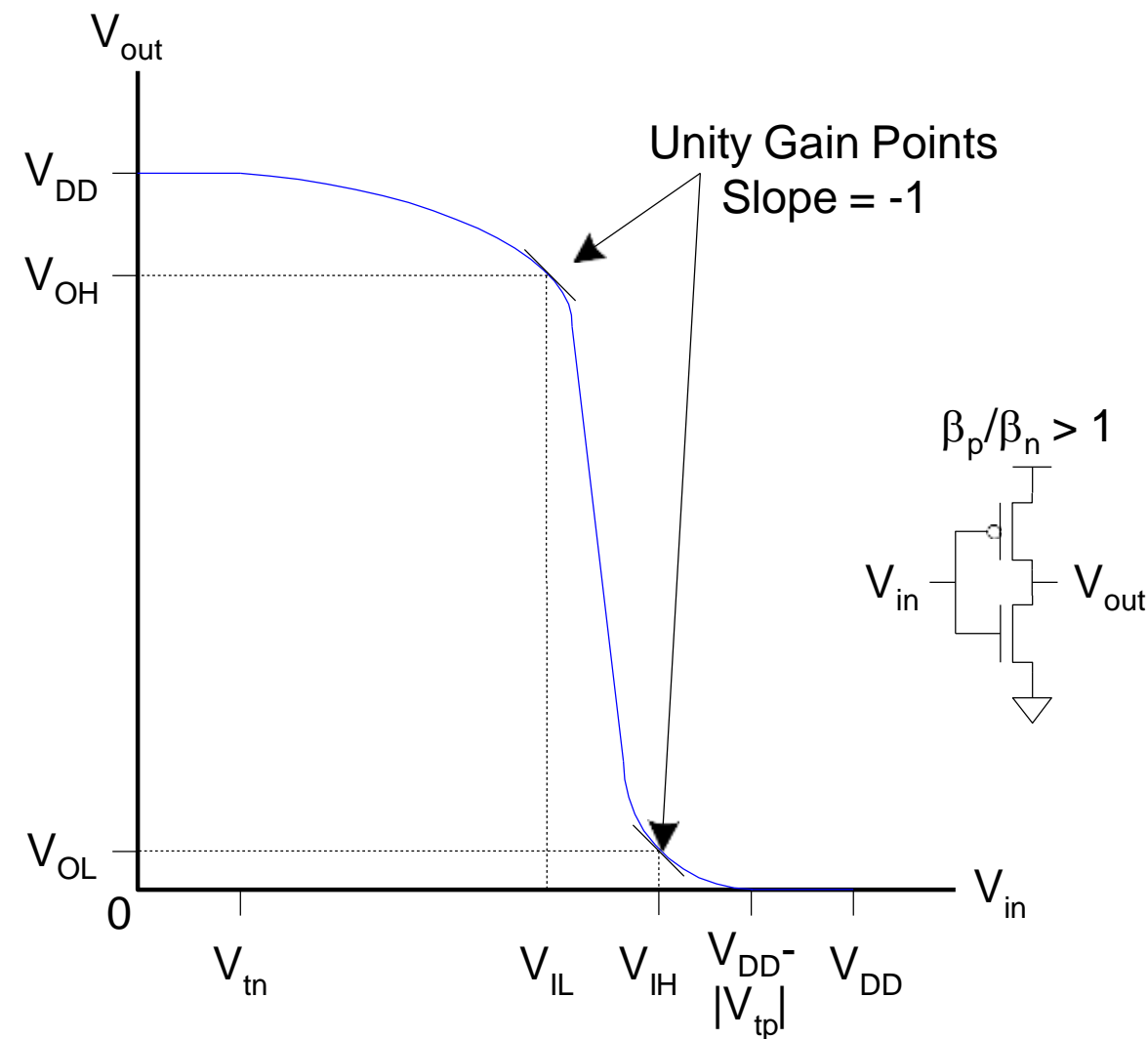




LOGIC LEVELS



To maximize noise margins, select logic levels at unity gain point of DC transfer characteristic

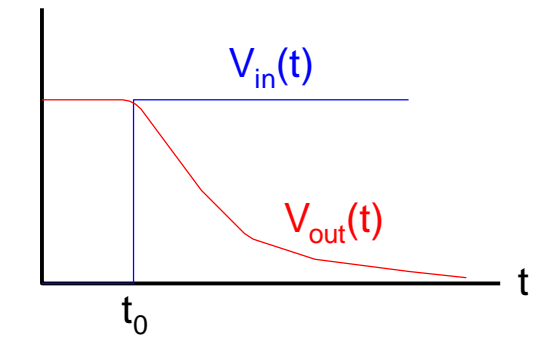
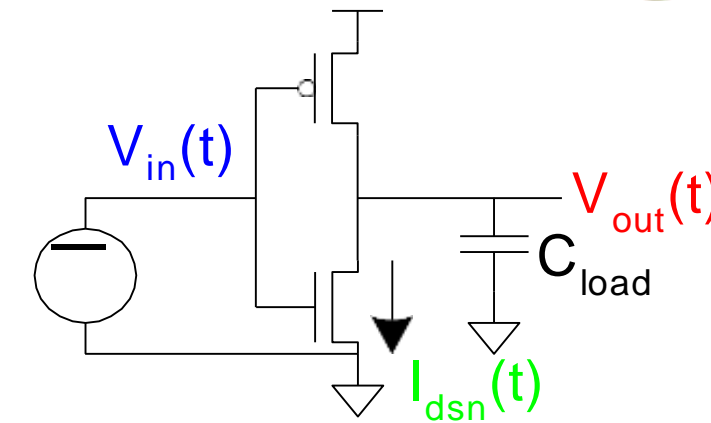




TRANSIENT RESPONSE



- DC analysis tells us V_{out} if V_{in} is constant
- Transient analysis tells us $V_{out}(t)$ if $V_{in}(t)$ changes
 - Requires solving differential equations
- Input is usually considered to be a step or ramp
 - From 0 to V_{DD} or vice versa



$$V_{in}(t) = u(t - t_0)V_{DD}$$

$$V_{out}(t < t_0) = V_{DD}$$

$$\frac{dV_{out}(t)}{dt} = -\frac{I_{dsn}(t)}{C_{load}}$$

$$I_{dsn}(t) = \begin{cases} 0 & t \leq t_0 \\ \frac{\beta}{2}(V_{DD} - V)^2 & V_{out} > V_{DD} - V_t \\ \beta\left(V_{DD} - V_t - \frac{V_{out}(t)}{2}\right)V_{out}(t) & V_{out} < V_{DD} - V_t \end{cases}$$



THANK YOU