



# SNS COLLEGE OF TECHNOLOGY

Coimbatore-35  
An Autonomous Institution



Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++' Grade (III Cycle)  
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

## DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

### 19ECB302-VLSI DESIGN

III YEAR/ V SEMESTER

#### UNIT 1 –MOS TRANSISTOR PRINCIPLE

#### TOPIC 7 –CMOS INVERETER DC CHARACTERISTICS

30 July 2024

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## OUTLINE



- INTRODUCTION
- DC RESPONSE
- LOGIC LEVELS AND NOISE MARGINS
- ACTIVITY
- TRANSIENT RESPONSE
- ASSESSMENT
- SUMMARY

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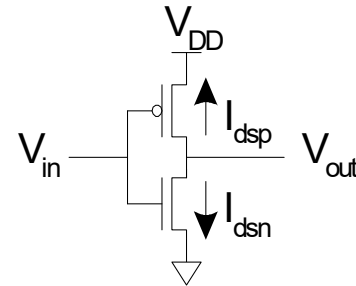
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## DC RESPONSE



- DC Response:  $V_{out}$  vs.  $V_{in}$  for a gate
- Ex: Inverter
  - When  $V_{in} = 0 \rightarrow V_{out} = V_{DD}$
  - When  $V_{in} = V_{DD} \rightarrow V_{out} = 0$
  - In between,  $V_{out}$  depends on transistor size and current
  - By KCL, must settle such that  $I_{dsn} = |I_{dsp}|$
  - We could solve equations
  - But graphical solution gives more insight



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## TRANSISTOR OPERATION



- Current depends on region of transistor behavior
- For what  $V_{in}$  and  $V_{out}$  are nMOS and pMOS in
  - Cutoff?
  - Linear?
  - Saturation?

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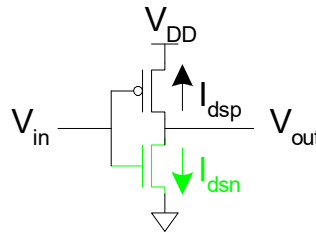
## NMOS OPERATION



Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$ $V_{in} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$ $V_{out} < V_{in} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$ $V_{out} > V_{in} - V_{tn}$

$$V_{gsn} = V_{in}$$

$$V_{dsn} = V_{out}$$



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## PMOS OPERATION

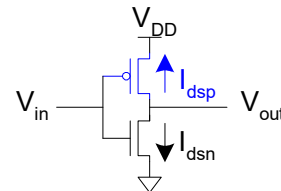


Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$ $V_{in} > V_{DD} + V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$

$$V_{gsp} = V_{in} - V_{DD}$$

$$V_{dsp} = V_{out} - V_{DD}$$

$$V_{tp} < 0$$



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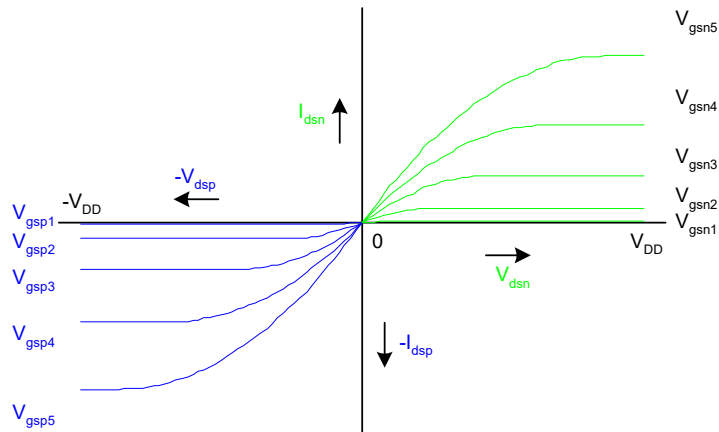
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## I-V CHARACTERISTICS



Make pMOS is wider than nMOS such that  $\beta_n = \beta_p$

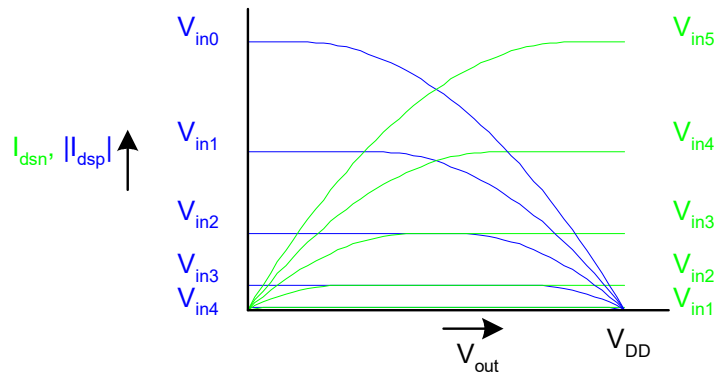


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## CURRENT VS $V_{OUT}$ , $V_{IN}$



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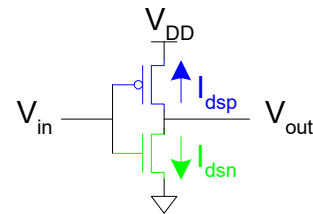
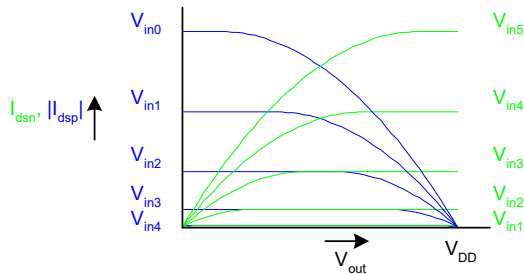
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## LOAD LINE ANALYSIS



- For a given  $V_{in}$ :
  - Plot  $I_{dsn}$ ,  $I_{dsp}$  vs.  $V_{out}$
  - $V_{out}$  must be where |currents| are equal in

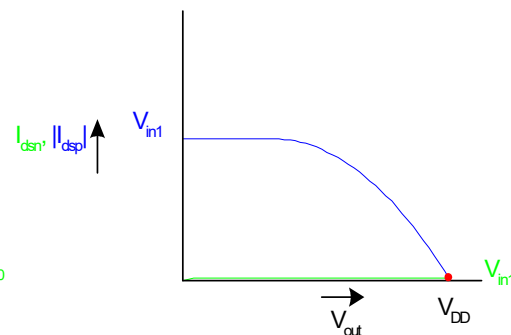
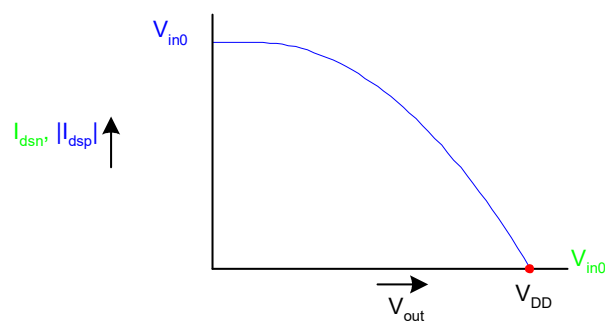


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## LOAD LINE ANALYSIS


 $V_{in} = 0$ 
 $V_{in} = 0.2V_{DD}$ 


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## ACTIVITY-BRAIN TEASERS



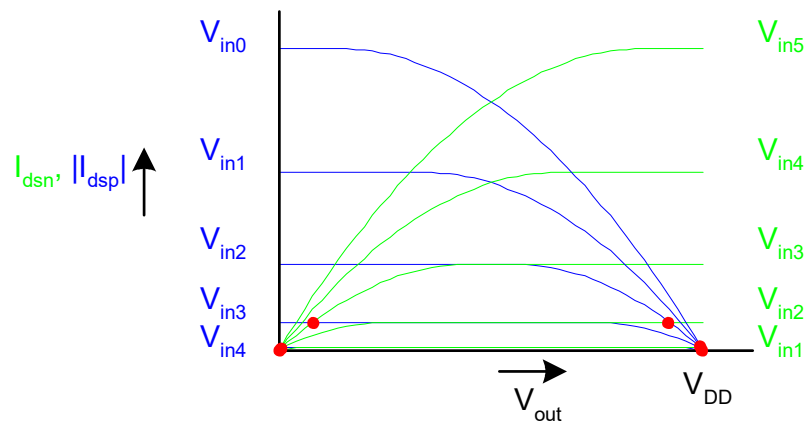
1 s a f e o r s y	2 <b>FUSS</b> ○	3 e d d e u n d c a k e	4 — T I K ○
5 o L D	6 T I L L I M E	7 <b>JOB</b> A N	8 W O R L D
9 P P O D	10 I N I T I A _	11 F I L E	12 J U S 1 4 4 T I C E
13 W O H N I C L E E	14 <b>L O V</b>	15 1 T 3 4 5 6	16 B R I N G B A L L E R I N A S

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## LOAD LINE ANALYSIS SUMMARY



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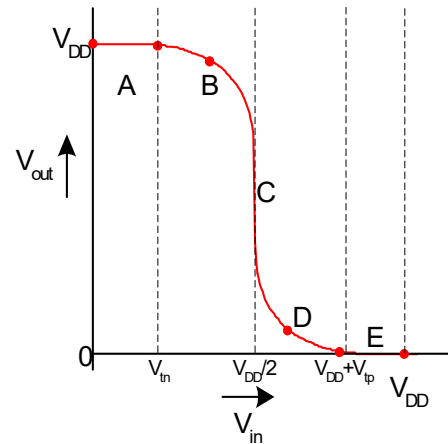
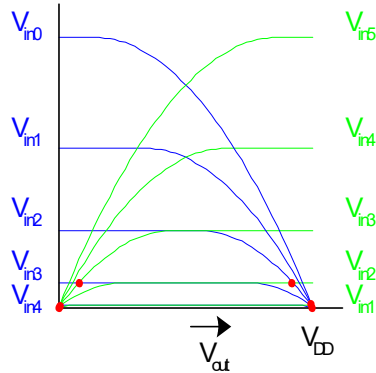
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## DC TRANSFER CURVE



Transcribe points onto  $V_{in}$  vs.  $V_{out}$  plot



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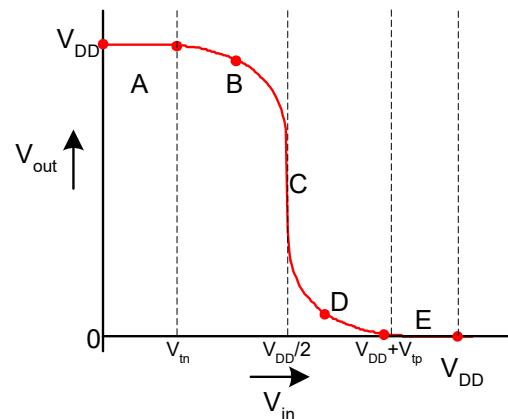
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## REVISIT TRANSISTOR OPERATING REGIONS



Region	nMOS	pMOS
A	Cutoff	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cutoff



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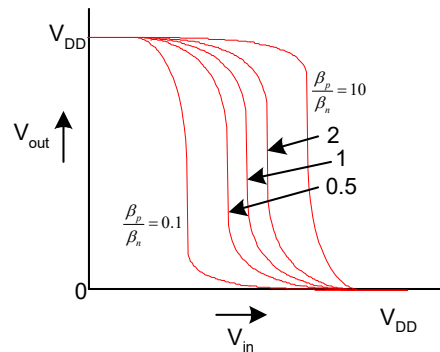
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## BETA RATIO



If  $\beta_p / \beta_n \neq 1$ , switching point will move from  $V_{DD}/2$ . Called skewed gate  
Other gates: collapse into equivalent inverter



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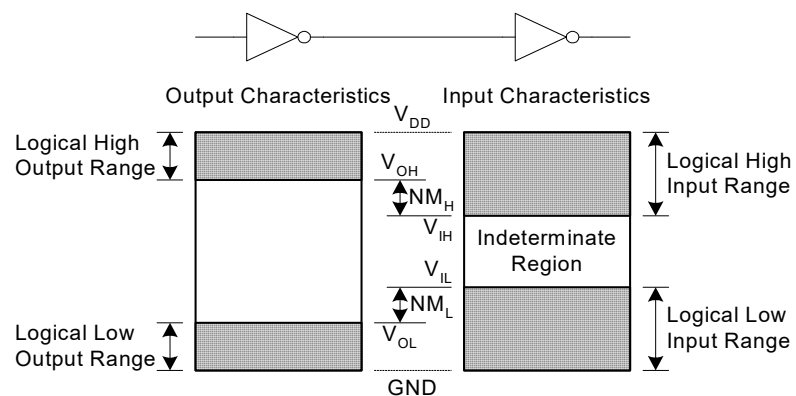
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## NOISE MARGINS



How much noise can a gate input see before it does not recognize the input?



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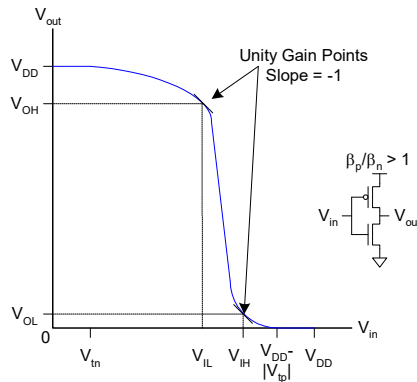




## LOGIC LEVELS



To maximize noise margins, select logic levels at unity gain point of DC transfer characteristic



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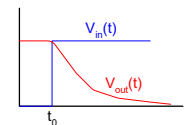
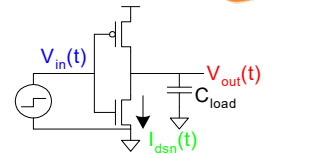
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## TRANSIENT RESPONSE



- DC analysis tells us  $V_{out}$  if  $V_{in}$  is constant
- Transient analysis tells us  $V_{out}(t)$  if  $V_{in}(t)$  changes
  - Requires solving differential equations
- Input is usually considered to be a step or ramp
  - From 0 to  $V_{DD}$  or vice versa



$$V_{in}(t) = u(t - t_0)V_{DD}$$

$$V_{out}(t < t_0) = V_{DD}$$

$$\frac{dV_{out}(t)}{dt} = -\frac{I_{dsn}(t)}{C_{load}}$$

$$I_{dsn}(t) = \begin{cases} 0 & t \leq t_0 \\ \frac{\beta}{2}(V_{DD} - V_t)^2 & V_{at} > V_{DD} - V_t \\ \beta \left( V_{DD} - V_t - \frac{V_{at}(t)}{2} \right) V_{at}(t) & V_{at} < V_{DD} - V_t \end{cases}$$

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## ASSESSMENT



- 1) If the width of a transistor increases, the current will  
increase      decrease      not change
- 2) If the length of a transistor increases, the current will  
increase      decrease      not change
- 3) If the supply voltage of a chip increases, the maximum transistor current will  
increase      decrease      not change
- 4) If the width of a transistor increases, its gate capacitance will  
increase      decrease      not change
- 5) If the length of a transistor increases, its gate capacitance will  
increase      decrease      not change
- 6) If the supply voltage of a chip increases, the gate capacitance of each transistor will  
increase      decrease      not change

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## ACTIVITY



- 1) If the width of a transistor increases, the current will  
**increase**      decrease      not change
- 2) If the length of a transistor increases, the current will  
increase      **decrease**      not change
- 3) If the supply voltage of a chip increases, the maximum transistor current will  
**increase**      decrease      not change
- 4) If the width of a transistor increases, its gate capacitance will  
**increase**      decrease      not change
- 5) If the length of a transistor increases, its gate capacitance will  
**increase**      decrease      not change
- 6) If the supply voltage of a chip increases, the gate capacitance of each transistor will  
increase      decrease      **not change**

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## SUMMARY & THANK YOU

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