



SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution



Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A+' Grade (III Cycle)
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB302-VLSI DESIGN

III YEAR/₁V SEMESTER

UNIT 2 –COMBINATIONAL LOGIC CIRCUITS

TOPIC 9 –Design for low power principles

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OUTLINE



- Power and Energy
- Dynamic Power Reduction
- Activity
- Static Power
- Low Power Design Principles
- Assessment
- Summary

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Power and Energy



- Power is drawn from a voltage source attached to the V_{DD} pin(s) of a chip.

- Instantaneous Power: $P(t) = i_{DD}(t)V_{DD}$

- Energy: $E = \int_0^T P(t)dt = \int_0^T i_{DD}(t)V_{DD}dt$

- Average Power: $P_{avg} = \frac{E}{T} = \frac{1}{T} \int_0^T i_{DD}(t)V_{DD}dt$



Dynamic Power Reduction



- Dynamic Power Reduction (P_d)

$$P_d = \alpha C V_{DD}^2 f_{clk}$$

f_{clk} ---> Clock Frequency

α ---> Activity factor

C ---> Switching Capacitance



Dynamic Power Reduction



- If the chip is active, dynamic power dissipation is high.
- P_d is reduced by reducing α , C , V_{DD} or f_{clk} .
- Clock gating is used to stop portions of the IC that are idle.
- Device switching capacitance can be reduced by using small transistors.
- Internet switching capacitance can be reduced by proper floor planning.
- If low power supply is used, then the power consumption is reduced
- When more transistors are operated in a velocity saturated region. So, the performance will not be reduced due to low power supply.

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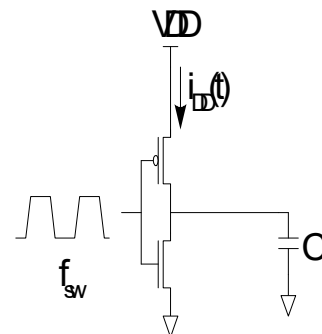
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Dynamic Power



- Dynamic power is required to charge and discharge load capacitances when transistors switch.
- One cycle involves a rising and falling output.
- On rising output, charge $Q = CV_{DD}$ is required
- On falling output, charge is dumped to GND
- This repeats Tf_{sw} times over an interval of T



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Dynamic Power Cont.



$$\begin{aligned}
 P_{\text{dynamic}} &= \frac{1}{T} \int_0^T i_{DD}(t) V_{DD} dt \\
 &= \frac{V_{DD}}{T} \int_0^T i_{DD}(t) dt \\
 &= \frac{V_{DD}}{T} [T f_{\text{sw}} C V_{DD}] \\
 &= C V_{DD}^2 f_{\text{sw}}
 \end{aligned}$$

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Activity Factor



Suppose the system clock frequency = f

Let $f_{\text{sw}} = \alpha f$, where α = activity factor

- If the signal is a clock, $\alpha = 1$
- If the signal switches once per cycle, $\alpha = \frac{1}{2}$
- Dynamic gates:
 - Switch either 0 or 2 times per cycle, $\alpha = \frac{1}{2}$
- Static gates:
 - Depends on design, but typically $\alpha = 0.1$

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Short Circuit Current



- When transistors switch, both nMOS and pMOS networks may be momentarily ON at once
- Leads to a blip of “short circuit” current.
- < 10% of dynamic power if rise/fall times are comparable for input and output

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Example



- 200 Mtransistor chip
 - 20M logic transistors
 - Average width: 12λ
 - 180M memory transistors
 - Average width: 4λ
- 1.2 V 100 nm process
- $C_g = 2 \text{ fF}/\mu\text{m}$

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Dynamic Example



- Static CMOS logic gates: activity factor = 0.1
 - Memory arrays: activity factor = 0.05 (many banks!)
 - Estimate dynamic power consumption per MHz.
- Neglect wire capacitance.

$$C_{\text{logic}} = (20 \times 10^6)(12\lambda)(0.05 \mu\text{m} / \lambda)(2 \text{ fF} / \mu\text{m}) = 24 \text{ nF}$$

$$C_{\text{mem}} = (180 \times 10^6)(4\lambda)(0.05 \mu\text{m} / \lambda)(2 \text{ fF} / \mu\text{m}) = 72 \text{ nF}$$

$$P_{\text{dynamic}} = [0.1C_{\text{logic}} + 0.05C_{\text{mem}}](1.2)^2 f = 8.6 \text{ mW/MHz}$$

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Activity



Genius Puzzle Series #4

THE CHESS PUZZLE

King + Knight + Bishop = 30
 Knight + Bishop + Pawn = 35
 Bishop + Pawn + Rook = 18
 Knight = Bishop = Pawn
 King + Rook × Bishop - Pawn = Queen
 Pawn = ?

what you think jerry?

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Static Power



- More static power is consumed by pseudo – n MOS gates.
- Static power is consumed even when chip is quiescent.
 - Ratioed circuits burn power in fight between ON
 - Transistors Leakage draws power from nominally OFF devices.
- Three parameters
 1. Supply Voltage
 2. Level Converter
 3. Capacitance

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Ratio Example



The chip contains a 32 word x 48 bit ROM
 Uses pseudo-nMOS decoder and bitline pullups
 one wordline and 24 bitlines are high

Find static power drawn by the ROM

$$\beta = 75 \mu\text{A}/\text{V}^2$$

$$V_{tp} = -0.4\text{V}$$

Solution

$$I_{\text{pull-up}} = \beta \frac{(V_{DD} - |V_{tp}|)^2}{2} = 24 \mu\text{A}$$

$$P_{\text{pull-up}} = V_{DD} I_{\text{pull-up}} = 29 \mu\text{W}$$

$$P_{\text{static}} = (31 + 24) P_{\text{pull-up}} = 1.6 \text{ mW}$$

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Leakage Example



- The process has two threshold voltages and two oxide thicknesses.
- Subthreshold leakage:
 - 20 nA/μm for low V_t
 - 0.02 nA/μm for high V_t
- Gate leakage:
 - 3 nA/μm for thin oxide
 - 0.002 nA/μm for thick oxide
- Memories use low-leakage transistors everywhere
- Gates use low-leakage transistors on 80% of logic



Leakage Example



- Estimate static power:

–High leakage: $(20 \times 10^6)(0.2)(12\lambda)(0.05 \mu\text{m} / \lambda) = 24 \times 10^6 \mu\text{m}$

$$I_{\text{static}} = (2.4 \times 10^6 \mu\text{m})[(20 \text{ nA} / \mu\text{m}) / 2 + (3 \text{ nA} / \mu\text{m})] +$$

$$(45.6 \times 10^6 \mu\text{m})[(0.02 \text{ nA} / \mu\text{m}) / 2 + (0.002 \text{ nA} / \mu\text{m})]$$

$$= 32 \text{ mA}$$

- Low leakage:

$$P_{\text{static}} = I_{\text{static}} V_{DD} = 38 \text{ mW}$$

$$(20 \times 10^6)(0.8)(12\lambda)(0.05 \mu\text{m} / \lambda) +$$

$$(180 \times 10^6)(4\lambda)(0.05 \mu\text{m} / \lambda) = 45.6 \times 10^6 \mu\text{m}$$

- if no low leakage devices, $P_{\text{static}} = 749 \text{ mW} (!)$



Low Power Design principles



Reduce dynamic power

- α : clock gating, sleep mode
- C: small transistors (esp. on clock), short wires
- V_{DD} : lowest suitable voltage
- f: lowest suitable frequency

Reduce static power

- Selectively use ratioed circuits
- Selectively use low V_t devices
- Leakage reduction:
 - stacked devices, body bias, low temperature



Assessment



- **Reduce dynamic power---?????????**
 - α :
 - C:
 - V_{DD} :
 - F:
- **Reduce static power-Fill up the blanks???**
 - Selectively use -----circuits
 - Selectively use low -----devices
 - ----- reduction:
 - devices, ----- bias,-----
temperature



THANK YOU