SNS COLLEGE OF TECHNOLOGY

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Coimbatore-35

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ITT204 - MICROCONTROLLER AND EMBEDDED SYSTEMS

III YEAR/ V SEMESTER

UNIT II PERIPHERAL INTERFACING

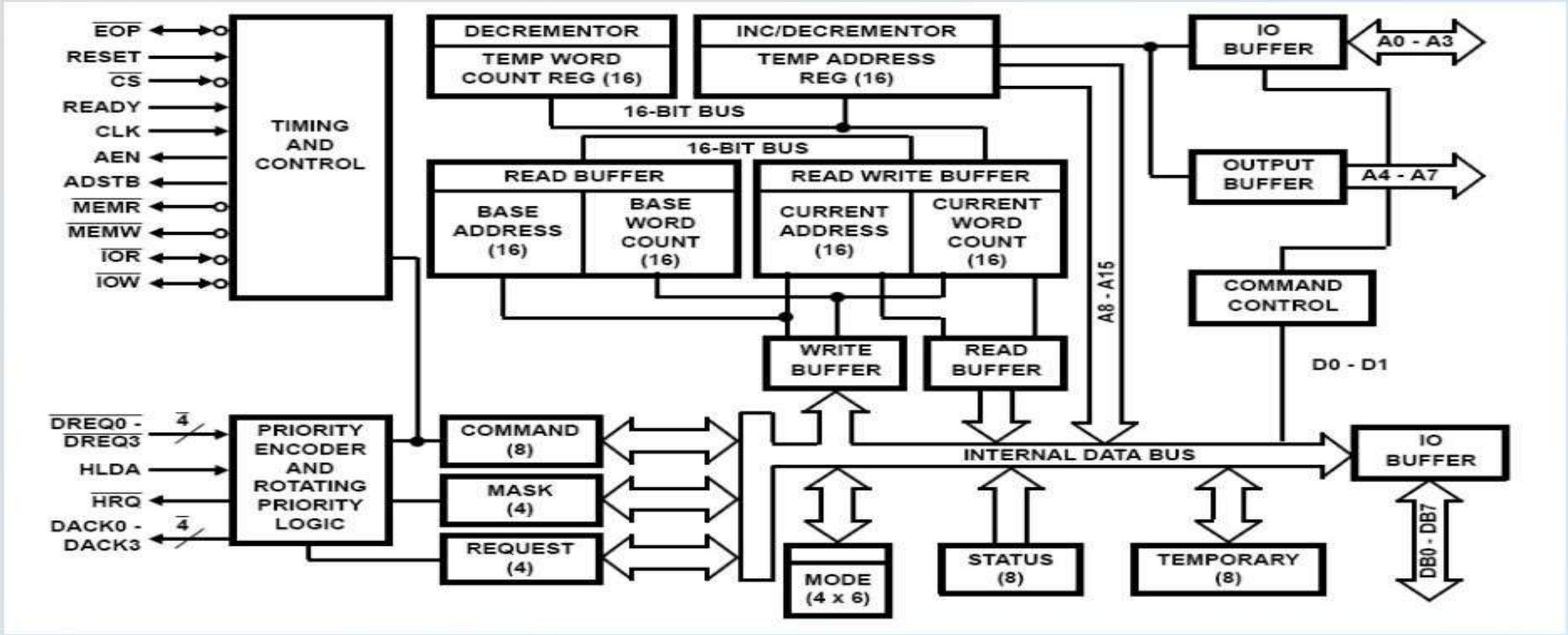
TOPIC – 8257 DMA Controller

OUTLINE

Introduction:

- Direct Memory Access (DMA) is a method of allowing data to be moved from one location to another in a computer without intervention from the central processor (CPU).
- It is also a fast way of transferring data within (and sometimes between) computer.
- The DMA I/O technique provides direct access to the memory while the microprocessor is temporarily disabled.
- The DMA controller temporarily borrows the address bus, data bus and control bus from the microprocessor and transfers the data directly from the external devices to a series of memory locations (and vice versa).

8237 block diagram

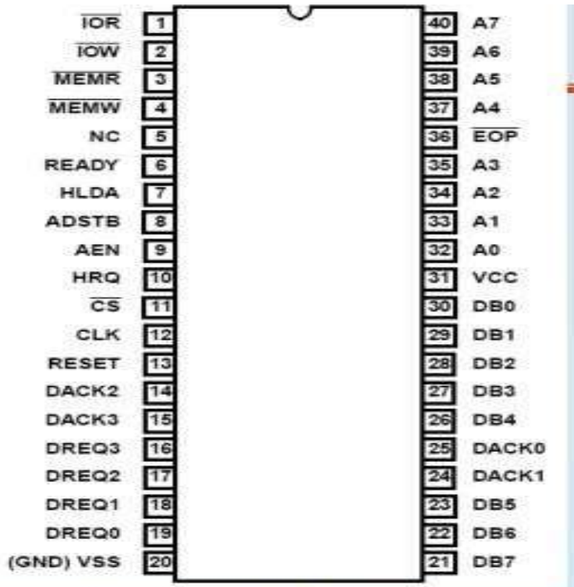


The 8237 DMA controller

- Supplies memory and I/O with control signals and addresses during DMA transfer
- 4-channels (expandable)
  - 0: DRAM refresh
  - 1: Free
  - 2: Floppy disk controller
  - 3: Free
- 1.6MByte/sec transfer rate
- 64 KByte section of memory address capability with single programming
- "fly-by" controller (data does not pass through the DMA-only memory to I/O transfer capability)
- Initialization involves writing into each channel:
  - i) The address of the first byte of the block of data that must be transferred (called the base address).
  - ii) The number of bytes to be transferred (called the word count).

8237 pins

- CLK: System clock
- CS´: Chip select (decoder output)
- RESET: Clears registers, sets mask register
- READY: 0 for inserting wait states
- HLDA: Signals that the µp has relinquished buses
- DREQ3 – DREQ0: DMA request input for each channel
- DB7-DB0: Data bus pins
- IOR´: Bidirectional pin used during programming and during a DMA write cycle
- IOW´: Bidirectional pin used during programming and during a DMA read cycle
- EOP´: End of process is a bidirectional signal used as input to terminate a DMA process or as output to signal the end of the DMA transfer
- A3-A0: Address pins for selecting internal registers
- A7-A4: Outputs that provide part of the DMA transfer address
- HRQ: DMA request output
- DACK3-DACK0: DMA acknowledge for each channel.
- AEN: Address enable signal
- ADSTB: Address strobe
- MEMR´: Memory read output used in DMA read cycle
- MEMW´: Memory write output used in DMA write cycle



Block Diagram Description

- It containing Five main Blocks.

1. Data bus buffer
2. Read/Control logic
3. Control logic block
4. Priority resolver
5. DMA channels.

DATA BUS BUFFER:

- It contain tristate ,8 bit bi-directional buffer.
- Slave mode ,it transfer data between microprocessor and internal data bus.
- Master mode ,the outputs A8-A15 bits of memory address on data lines (Unidirectional).

READ/CONTROL LOGIC:

- It control all internal Read/Write operation.
- Slave mode ,it accepts address bits and control signal from microprocessor.
- Master mode ,it generate address bits and control signal.

Control logic block

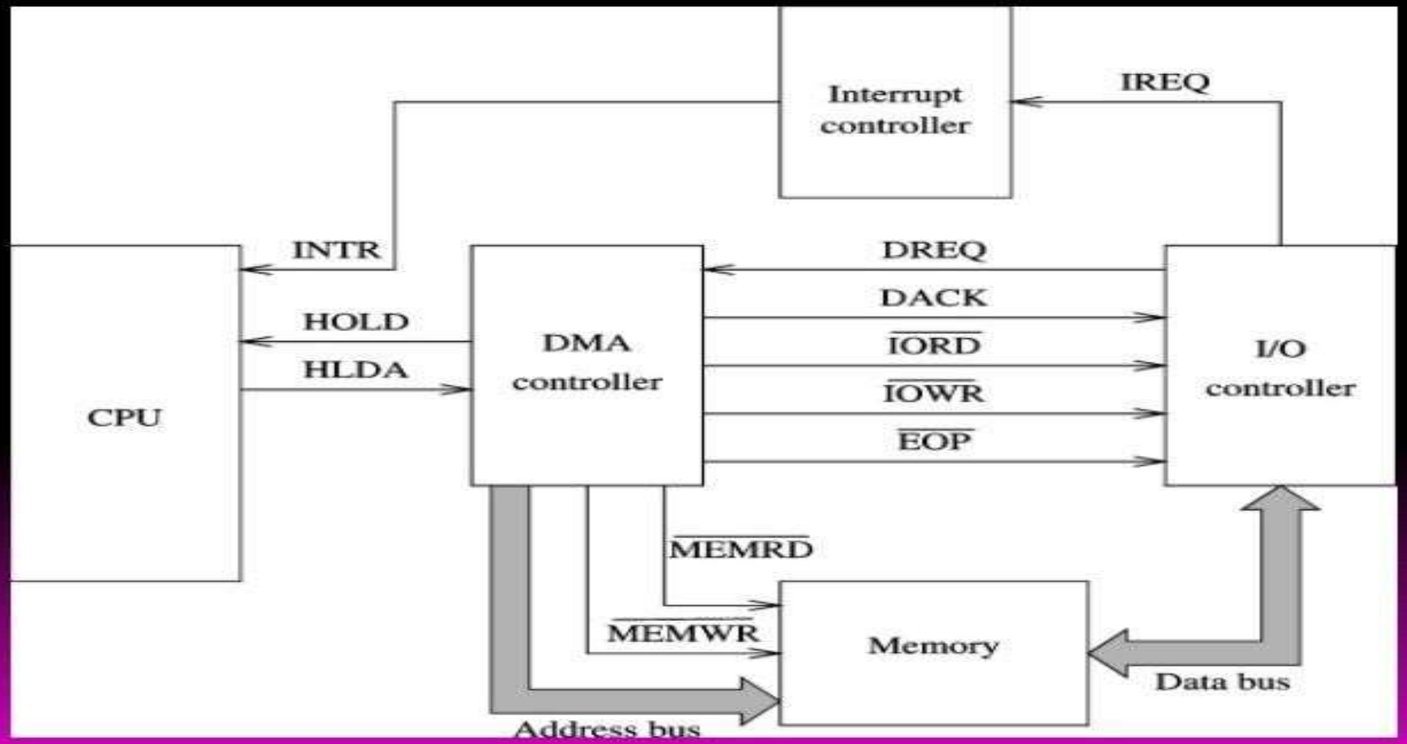
- It contains ,

1. Control logic
2. Mode set register and
3. Status Register.

CONTROL LOGIC:

- Master mode ,It control the sequence of DMA operation during all DMA cycles.
- It generates address and control signals.
- It increments 16 bit address and decrement 14 bit counter registers.
- It activate a HRQ signal on DMA channel Request.
- Slave ,mode it is disabled.

DMA controller details



THANK YOU