



SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)

Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai

Accredited by NAAC-UGC with 'A++' Grade (Cycle III) &

Accredited by NBA (B.E - CSE, EEE, ECE, Mech & B.Tech.IT)

COIMBATORE-641 035, TAMIL NADU



Reg. No:

B.E/B.Tech- Internal Assessment – I
Academic Year 2024-2025 (ODD Semester)
Fifth Semester
Artificial Intelligence and Machine Learning
23ITT202 – Computer Organization and Architecture
Answer Key



Time: 1^{1/2} Hours

Maximum Marks: 50

Answer All Questions

	PART – A (5*2 = 10 Marks)	CO	Blooms												
1.	<p>Write a program that can evaluate the expression $A*B+C*D$ in a single- accumulator processor. Assume that the processor has load, store, multiply and add instruction and that all value fit in the accumulator.</p> <p>Load A Multiply B Store RESULT Load C Multiply D Add RESULT Store RESULT</p>	CO1	APP												
2.	<p>Given a binary pattern in some memory location, is it possible to tell whether this pattern represents a machine instruction or a number?</p> <p>No; any binary pattern can be interpreted as a number or as an instruction.</p>	CO1	UND												
3.	<p>Difference between little- endian and big-endian assignments.</p> <table border="1"> <thead> <tr> <th>Big Endian</th> <th>Little Endian</th> </tr> </thead> <tbody> <tr> <td>Easier to determine Sign of a number</td> <td>Easier addition & multiplication of multiprecision number</td> </tr> <tr> <td>Easier to compare two numbers</td> <td>Requires more number of comparisons for comparing two numbers</td> </tr> <tr> <td>Easier to divide two numbers</td> <td></td> </tr> <tr> <td>Easier to print</td> <td></td> </tr> <tr> <td>MOTOROLA, IBM systems, TCP/IP</td> <td>Intel Systems, RS-232, AMD</td> </tr> </tbody> </table>	Big Endian	Little Endian	Easier to determine Sign of a number	Easier addition & multiplication of multiprecision number	Easier to compare two numbers	Requires more number of comparisons for comparing two numbers	Easier to divide two numbers		Easier to print		MOTOROLA, IBM systems, TCP/IP	Intel Systems, RS-232, AMD	CO1	UND
Big Endian	Little Endian														
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4.	<p>Consider 5-bit signed number -14 and 11 and perform binary addition</p> <p>2's Complement of -3 = 11101 Signed Magnitude of -3= 10011</p>	CO2	APP												
5.	<p>Sketch the binary addition and subtraction logic Network</p>	CO2	UND												

PART – B (2*13=26 Marks) & (1*14=14 Marks)

				CO	Blooms
6.	(a)	<p>(i) Summarize the functional units of computer by extending the basic operational concepts. Block Diagram – 2 marks Functional Unit Explanation – 3 mark Basic Operational Concepts – 2 mark</p>		7	CO1 UND

		<p>(ii) Explain in detail about different instruction types and instruction sequencing with your own example. Basic instruction types-4 types + Explanation – 3marks</p> <ul style="list-style-type: none"> • Zero address instruction • One address instruction • Two address instruction • Three address instruction <p>Instruction Sequencing – 3 Ma</p>		6	CO1 UND
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(OR)

	(b)	<p>Define addressing mode and explain the basic addressing modes with an example for each.</p> <p>Definition – 2 marks Types – 3 marks Explanation & Diagram – 8 marks</p>		13	CO1 UND
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7. (a) **Explain the concept of addition and subtraction of signed numbers with algorithm and examine the usage of each level in a problem**
 Algorithm +Explanation - 12 Marks (each 6 marks)
 Diagram – 1 mark

Subtract

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graph TD
    A[Minuend in AC  
Subtrahend in B] --> B[AC ← AC + B' + 1  
V ← overflow]
    B --> C[END]
            
```

Add

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graph TD
    A[Augend in AC  
Addend in B] --> B[AC ← AC + B  
V ← overflow]
    B --> C[END]
            
```

Operation	Add Magnitude	Subtract Magnitude		
		When A>B	When A<B	When A=B
(+A) + (+B)	+(A + B)	+(A - B)	-(B - A)	+(A - B)
(+A) + (-B)	-(A + B)	-(A - B)	+(B - A)	+(A - B)
(-A) + (+B)	-(A + B)	+(A - B)	-(B - A)	+(A - B)
(-A) + (-B)	+(A + B)	-(A - B)	+(B - A)	+(A - B)

(OR)

(b) **Illustrate the concept of Carry Look Ahead Adder with diagram.**
 Definition – 2 marks
 Diagram – 2 marks
 Explanation (Advantage & Disadvantage) – 5 marks
 Derivation – 4 marks

$$C_1 = G_0 + P_0 \cdot C_0$$

$$C_2 = G_1 + P_1 \cdot C_1 = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_0$$

$$C_3 = G_2 + P_2 \cdot C_2 = G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_0$$

$$C_4 = G_3 + P_3 \cdot C_3 = G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 + P_3 \cdot P_2 \cdot P_1 \cdot P_0 \cdot C_0$$

$$C_{i+1} = G_i + P_i \cdot G_{i-1} + P_i \cdot P_{i-1} \cdot C_{i-1}$$

8. (a) **i) Registers R1 and R2 of a computer contain the decimal values 1200 and 4600. In each of the following instructions determine the Addressing mode used in the instruction and find the effective address of the memory operand?**

- Load 20(R1),R5
- Move #3000,R5
- Store R5,30(R1,R2)
- Add -(R2),R5
- Subtract (R1)+,R5

1220, part of the instruction, 5830, 4599, 1200

ii) Register r5 is used in a program to point to the top of a stack. Write a sequence of instruction using index, auto increment and auto decrement addressing modes to perform each of the following tasks

- Pop the top two items off the stack, add them, and then push the result onto the stack
- Copy the fifth item from the top into register R3
- Remove the top ten items from the stack

- Move (R5)+,R0
Add (R5)+,R0
Move R0,-(R5)
- Move 16(R5),R3
- Add #40,R5

(OR)

	<p>(b) i) Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 250 ps and a CPI of 2.0 for some program, and computer B has a clock cycle time of 500 ps and a CPI of 1.2 for the same program. Which computer is faster for this program and by how much?</p> <p style="text-align: center;">Computer A is 1.2 times as fast as computer</p>	7	CO1	APP
	<p>ii) Our favorite program runs in 10 seconds on computer A, which has a 2 GHz clock. We are trying to help a computer designer build a computer, B, which will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer B to require 1.2 times as many clock cycles as computer A for this program. What clock rate should we tell the designer to target?</p> <p>Clock Rate_B = 4 GHz To run the program in 6 seconds, B must have twice the clock rate of A</p>	7	CO1	APP

Bloom's Taxonomy:

REM – Remember **UND** – Understand **APP**– Apply **ANA**– Analyze **EVA** - Evaluate

CRT - Create

Faculty in-charge Teaching Coordinator

HoD

Dean