Basic Mos transistors:-

nmos enhancement and depletion mode transistors:-

→ nmos devices are formed in a P-type substrate of moderate doping level.

→ The source and drain regions are formed by diffusing n-type impurities through suitable masks into these areas to give the desired n- impurity concentration and give rise to depletion regions which extend mainly in the more lightly doped P- region.

→ Thus source and drain are isolated from one another by 2 diodes.

→ connections to the source and drain are made by a deposited metal layer.

→ In order to make a useful device, there must be the capability to establishing and controlling a current b/w source and drain.

→ This is achieved in one of 2 ways, giving rise to the enhancement mode and depletion mode transistors.

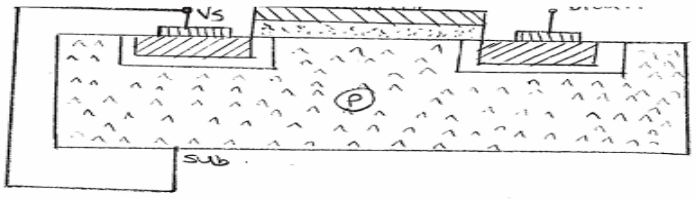
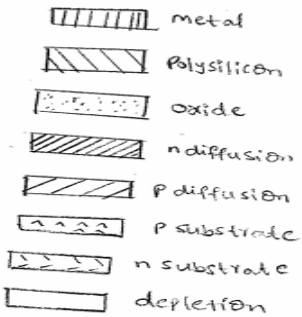


fig: nmos enhancement mode transistor



In the enhancement mode, A polysilicon gate is deposited on a layer of insulation over the region b/w source and drain.

→ In enhancement mode device the channel is not established and the device is in a non-conducting condition, $V_D = V_S = V_{GS} = 0$.

→ If the gate is connected to a suitable positive voltage with respect to source, then the electric field established b/w the gate and substrate give rise to a charge inversion region in the substrate under the gate insulation and a conducting path or channel is formed b/w source and drain.

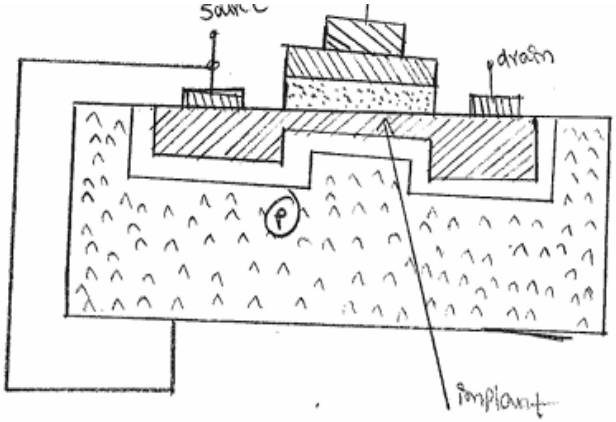
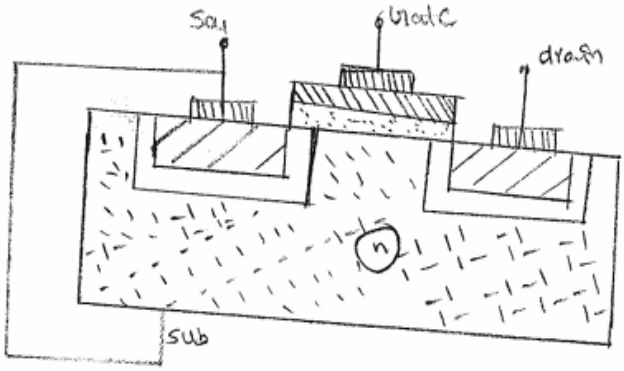


fig : nmos depletion mode transistor

In depletion mode, the channel may also be established so that it is present under the condition $V_{gs} = 0$ by implanting suitable impurities in the region b/w source and drain during manufacture and prior to depositing the insulation and the gate. Under these circumstances, source and drain are connected by a conducting channel, but the channel may now be closed by applying a suitable negative voltage to the gate.

In both cases, variations of the gate voltage allow control of any current flow b/w source and drain.



In Pmos enhancement mode Transistor, the substrate is "n" n-type material and the source and drain diffusions are p-type. By the application of a negative voltage of suitable magnitude ($>|V_t|$) b/w gate and source will rise to the formation of a channel (p-type) b/w source and drain and current may then flow if the drain is made negative with respect to the source.

→ In this case, the current is carried by holes as opposed to es.

→ The Pmos transistors are inherently slower than nmos, since $\mu_n = 2.5\mu_p$.

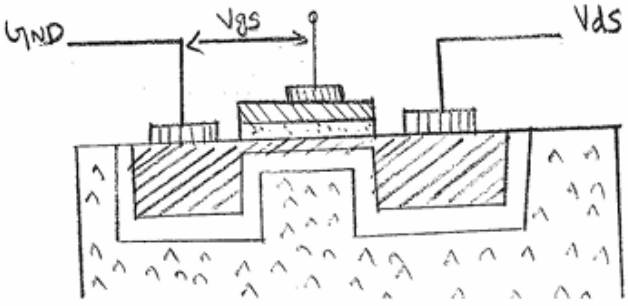
$\mu_n = 650\ cm^2/Vsec$

$\mu_p = 240\ cm^2/Vsec$.

Enhancement mode Transistor Action:

To understand the mechanism of Enhancemed mode we have to consider 3 conditions.

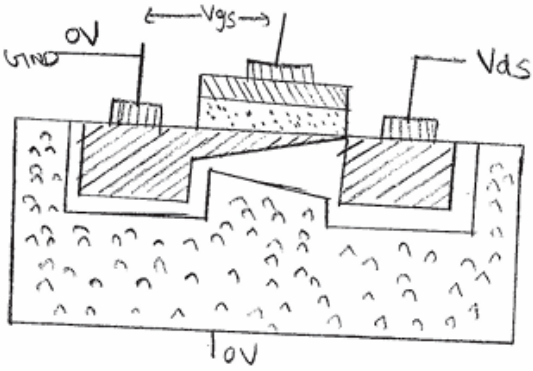
Threshold voltage (V_t):- The minimum voltage applied b/w gate and source to establish channel.



$V_{gs} > V_t$

$V_{ds} = 0V$

Fig. indicates the conditions prevailing with the channel established but no current flowing b/w source and drain ($V_{ds} = 0$).



$V_{gs} > V_t$

$V_{ds} < V_{gs} - V_t$

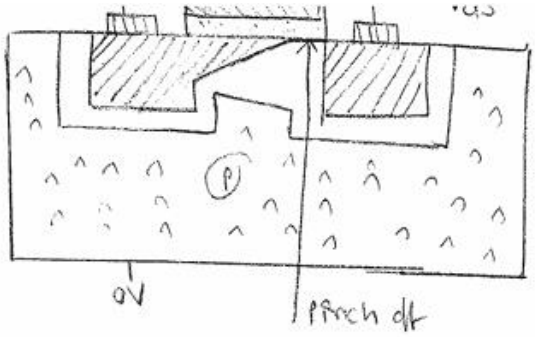
→ Now consider the conditions prevailing when current flows in the channel by applying a voltage V_{ds} b/w drain and source.

→ Along the channel, a corresponding IR drop = V_{ds} will be there.

→ This results in the voltage b/w gate and channel varying with distance along the channel with the voltage being a maximum of V_{gs} at the source end.

→ Since the effective gate voltage is $V_g = V_{gs} - V_t$ (no current flows when $V_{gs} < V_t$), there will be voltage available to invert the channel at the drain end so long as $V_{gs} - V_t \geq V_{ds}$.

→ The limiting condition comes when $V_{ds} = V_{gs} - V_t$. For all voltages $V_{ds} < V_{gs} - V_t$, the device is in the non-saturation region of operation which is $\boxed{V_{ds} < V_{gs} - V_t}$.



If Vds is increased to a level greater than $V_{gs}-V_t$. In this case, an IR drop = $V_{gs}-V_t$ takes place over less than the whole length of the channel so that over part of the channel, near the drain, there is insufficient electric field available to give rise to an inversion layer to create the channel. The channel is therefore "pinch-off".

→ Diffusion current completes the path from source to drain in this case, causing the channel to exhibit a high resistance and behave as a constant current source.

→ This region is known as saturation, is characterized by almost constant current for increase of Vds above $V_{ds} = V_{gs}-V_t$.

→ In all the cases the channel will cease to exist and no current will flow when $V_{gs} < V_t$.

→ The typical values for enhancement mode devices

$V_t = 1V$ for $V_{DD} = 5V$

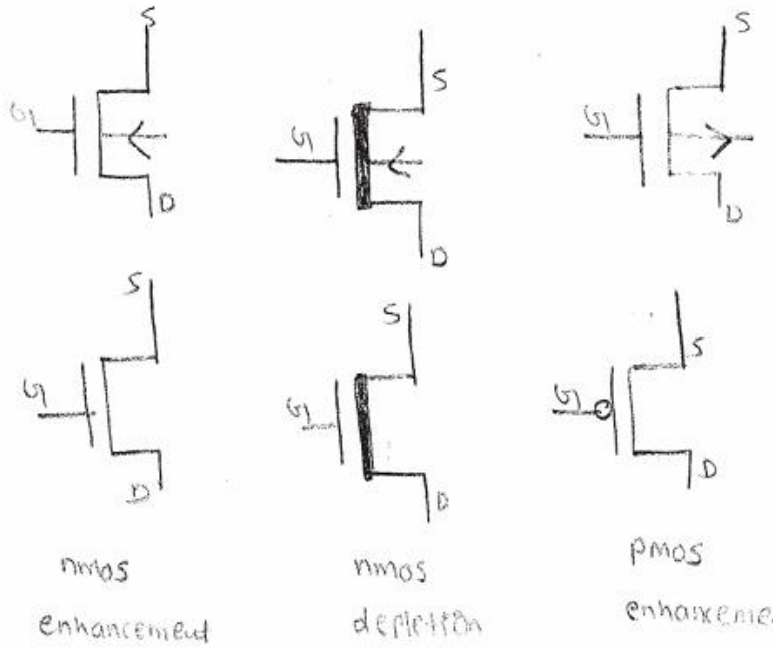
∴ In general $V_t = 0.2\,V_{DD}$.

Depletion mode transistor Action:-

For depletion mode device the channel is established because of the implant. even when $V_{gs} = 0$ and to cause the channel to cease to exist a negative voltage V_{td} must be applied b/w gate and source.

V_{td} is typically $\angle -0.8 V_{DD}$, depending on implant and substrate bias, but threshold voltage difference aside the action is simpler to that of enhancement mode T&R.

Symbols for nmos & pmos transistors:



nmos enhancement

nmos depletion

pmos enhancement