SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)

COIMBATORE-35

Accredited by NBA-AICTE and Accredited by NAAC – UGC with A+ Grade

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

23EET202 / DIGITAL ELECTRONICS AND INTEGRATED CIRCUITS

II YEAR / IV SEMESTER

UNIT-I

DESIGN OF COMBINATIONAL CIRCUITS

TOPIC OUTLINE

Combinational circuits

Design Procedure

Half Adder Design

Full Adder Design

Multiplexer Design

Examples..

COMBINATIONAL CIRCUITS

- Adders
- Subtractors
- Multiplexers / De multiplexers
- Encoders / Decoders
- Code converters
- Magnitude comparators

DESIGN PROCEDURE

1. Read the question carefully, find number of inputs and outputs
2. Assign literals for the inputs/outputs
3. Develop the truth table as per question
4. Using k map, minimize the boolean expression
5. Draw logic circuit as per expression

DESIGN HALF ADDER

- The half adder:
  - The half adder is a circuit for adding two single bit numbers
  - Develop a truth table and Boolean expressions for the half adder

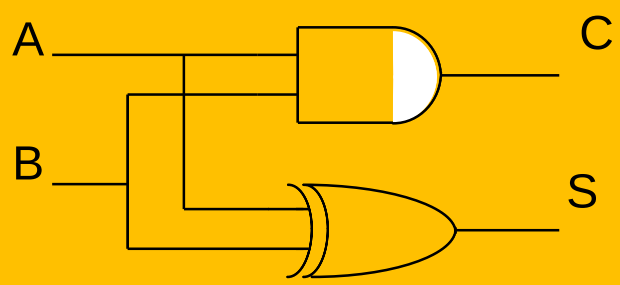
Truth table: S and C are the Sum and Carry

A	B	S	C
0	0		
0	1		
1	0		
1	1		

DESIGN HALF ADDER

- The sum is XOR operation and the carry an AND:

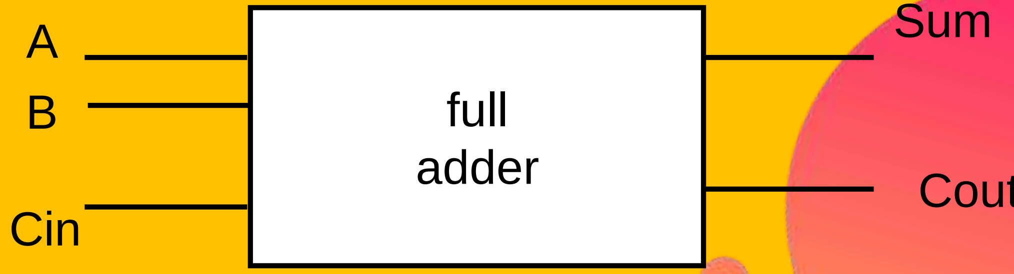
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



DESIGN OF FULL ADDER

- The full adder:
  - Develop a truth table and Boolean expressions for the full adder, this circuit also includes a carry in.

Cin	A	B	S	C
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		



DESIGN OF FULL ADDER

Cin	A	B	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth table

Exercise:

Complete the Karnaugh maps for the Sum and the Carry out columns

DESIGN OF FULL ADDER

Sum – 1 when odd number of inputs is 1 = XOR gate

Cin \ AB	00	01	11	10
0		1		1
1	1		1	

Sum = Cin xor A xor B

Carry out - simplifies to 3 pairs

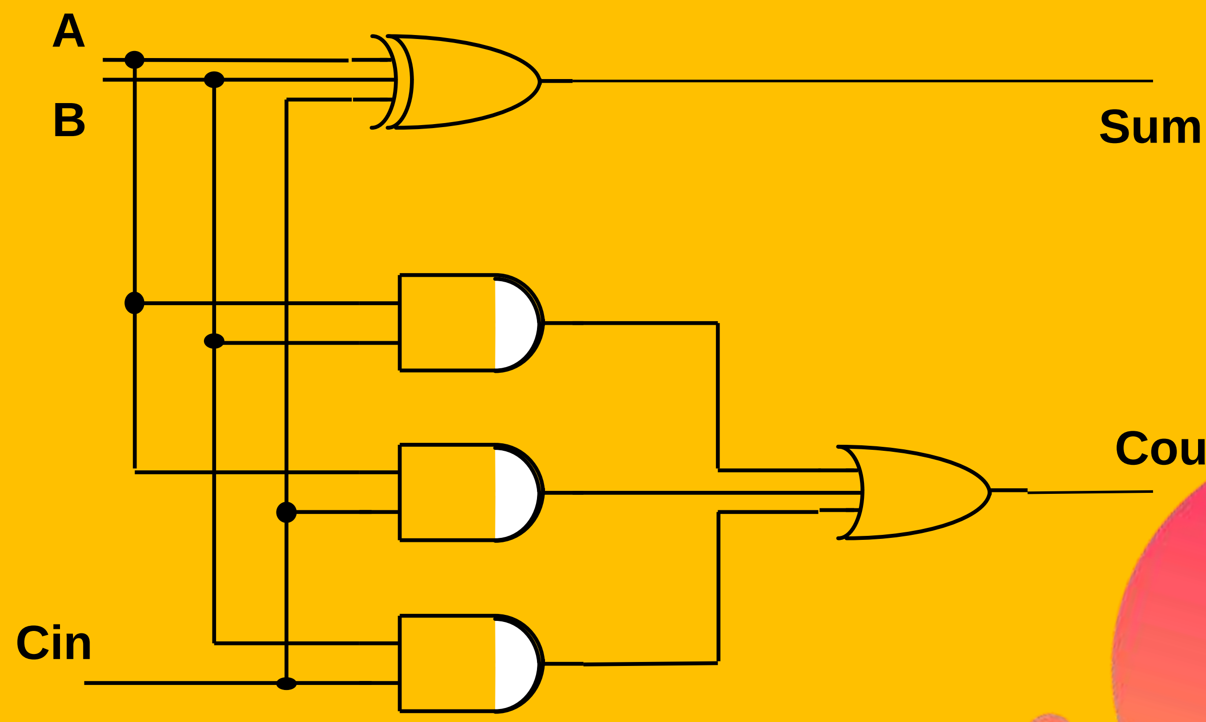
Cin \ AB	00	01	11	10
0			1	
1		1	1	1

Cout = A.B + A.Cin + B.Cin

K maps for sum and carry

DESIGN OF FULL ADDER

Full adder circuit

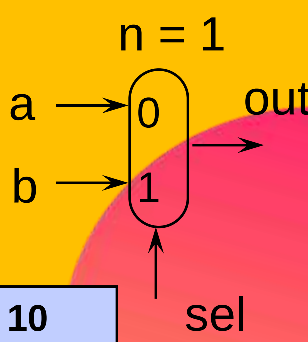


Sum = Cin xor A xor B

Cout = A.B + A.Cin + B.Cin

MULTIPLEXER

- The Multiplexer:
  - Selects one of 2^n inputs and copies it to a single output
  - The selected line is determined from the bit combination (address) on the n selection lines
  - e.g. 1 from 2 mutiplexer



sel	a	b	out
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

sel \ ab	00	01	11	10
0				
1				

out =

MULTIPLEXER

2:1 Multiplexer

sel	a	b	out
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

sel	a	b	out
0	0	?	0
0	1	?	1
1	?	0	0
1	?	1	1

if a is selected, don't care about b.

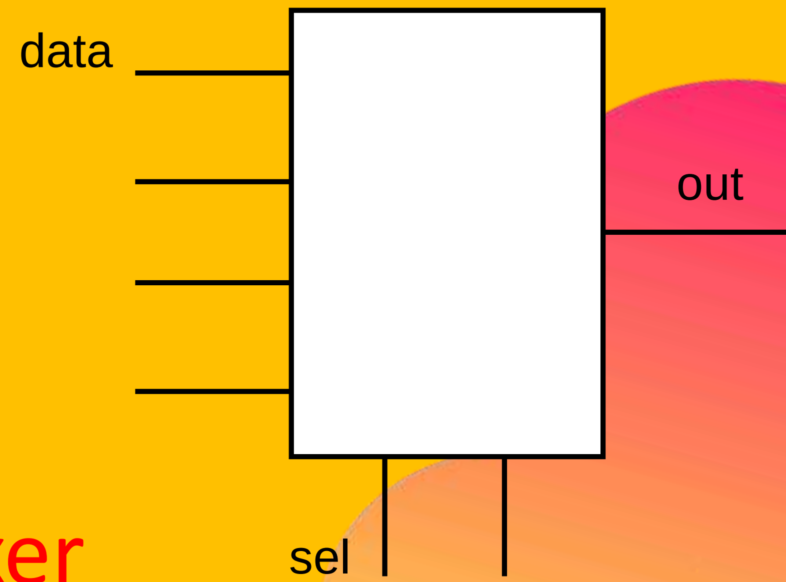
AB

sel	00	01	11	10
0			1	1
1		1	1	

MULTIPLEXER

AB / sel	00	01	11	10
0			1	1
1		1	1	

$$output = \overline{sel}.a + sel.b$$



Principal can be extended to

4:1 – 2 select lines and 4 data lines

8:1 – 3 select lines and 8 data lines

and so on…

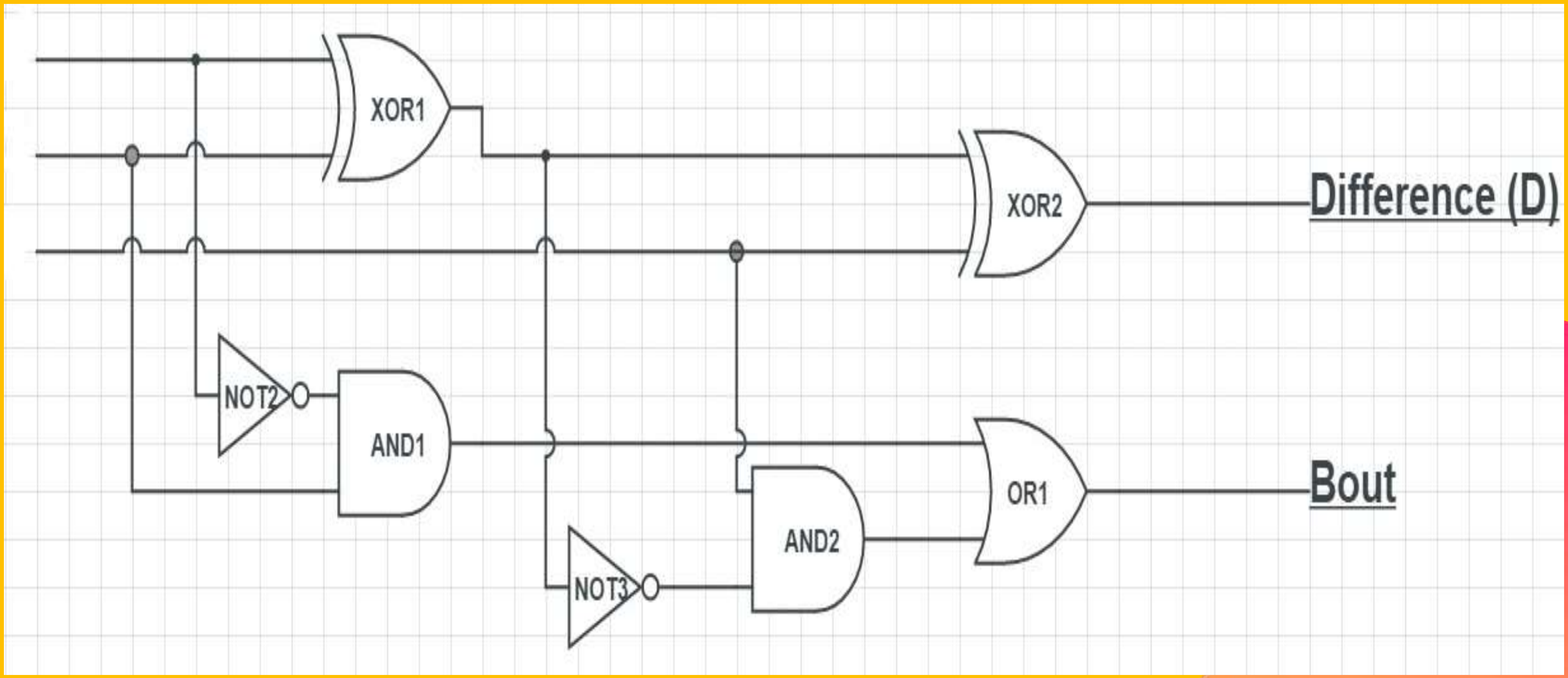
K map for 2:1 Multiplexer

DESIGN - PROBLEMS

Half Subtractor-Truth Table			
Input		Output	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Full Subtractor-Truth Table				
Input			Output	
A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

DESIGN - PROBLEMS



SUMMARIZE

More Design

Examples..

...code converters (4)

THANK YOU