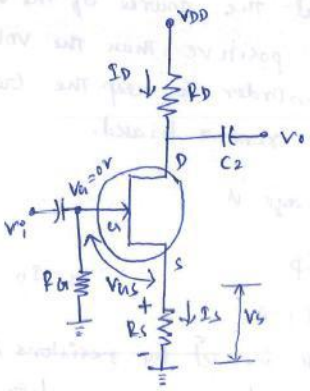
Topic 1.8 : FET- Self Bias configuration

3. Self Bias



* The Gate - Source junction is always reverse biased.
* The condition requires negative V_{GS} for n-channel JFET & a positive V_{GS} for p-channel JFET.
* The R_G does not affect the bias because it has essentially no voltage drop across it.
* ∴ The Gate remains at 0V.
* The voltage drop across resistor R_S make the Gate - Source junction reverse biased.
* Is produces voltage drop across R_S & make the source positive w.r.to ground.

Since

$$I_S = I_D \text{ & } V_G = 0 \quad \text{Then} \quad V_S = I_S R_S = I_D R_S$$

* The Gate - Source Voltage is

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$$

For p channel :

* The voltage drop across R_S & make the source negative w.r.t ground.

Since

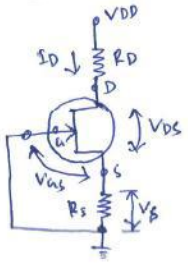
$$I_S = I_D \text{ & } V_G = 0 \quad \text{Then} \quad V_S = -I_S R_S = -I_D R_S$$

* The Gate - Source Voltage is

$$V_{GS} = V_G - V_S = 0 - (-I_D R_S) = I_D R_S$$

DC Analysis:

For n-channel



For dc analysis the coupling capacitors are replaced by open circuit & R_G is replaced by short circuit equivalent, since $I_G = 0$.

W.K.T

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad -(1)$$

Substitute the value of V_{GS} in eqn ①

① $\Rightarrow$ $I_D = I_{DSS}\left(1 - \frac{(-I_D R_S)}{V_P}\right)^2$ → for n-channel

$= I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$

Apply KVL to the Drain to source junction

$V_S + V_{DS} + I_D R_D - V_{DD} = 0$

$\therefore V_{DS} = V_{DD} - V_S - I_D R_D$

$= V_{DD} - I_D R_S - I_D R_D$

$\therefore V_{DS} = V_{DD} - I_D(R_S + R_D)$