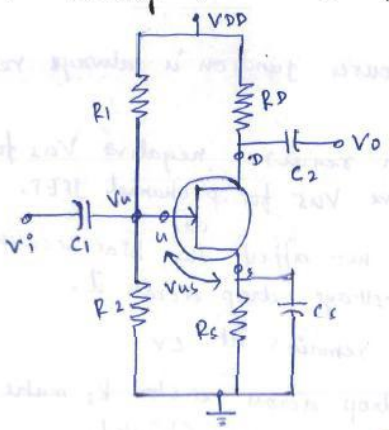
Topic 1.9 : FET –Voltage divider Bias configuration

2. Voltage Divider Bias / potential Divider Bias



* The voltage at the source of the JFET must be more positive than the voltage at the Gate in Order to keep the Gate - Source junction reverse biased.

* The source voltage is

$$V_S = I_S R_S \qquad \because I_S = I_D$$

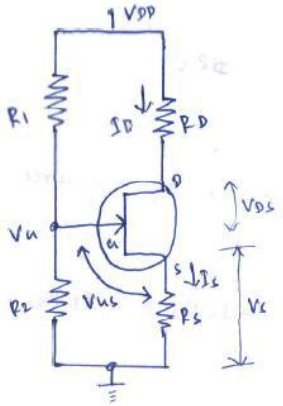
$$V_S = I_D R_S$$

* The Gate voltage is set by resistors R_1 & R_2 as expressed by the following equation using The voltage divider formula

$$V_G = \left(\frac{R_2}{R_1+R_2}\right) V_{DD} \qquad \because I_G = 0$$

Dc Analysis :

* For dc analysis the coupling capacitors are open circuited



* Apply KVL to the Gate - Source junction

$$V_{in} - V_{GS} - V_S = 0$$

$$V_{GS} = V_{in} - V_S$$

$$= V_{in} - I_S R_S \qquad \because I_S = I_D$$

$$= V_{in} - I_D R_S$$

$$\therefore V_{GS} = V_{in} - I_D R_S$$

* Apply KVL to the Drain - Source junction.

$$V_{DS} + I_D R_D + V_S - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D - \underset{\uparrow}{I_D R_S}$$ (V_S)

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

Q-point :

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$V_{DSQ} = V_{DD} - I_{DQ}(R_D + R_S)$$