Topic 1.7 : Biasing the FET & Fixed Bias configuration

Design of biasing for JFET

* FET - Field Effect Transistor - It's a semiconductor device which depends for its operation on the control of current by an electric field.

FET

- Junction field Effect Transistor (or) FET
- Metal - oxide - semiconductor Transistor (MOSFET)

FET differs from the BJT in the following characteristics

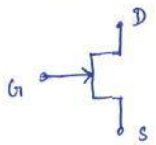
1. It's operation depends upon the flow of majority carriers only.
2. It's simpler to fabricate & occupies less space.
3. It exhibits a high input resistance, typically many megaohms.
4. It's less noisy compared to BJT.
5. It exhibits no offset voltage at zero drain current

Disadvantages of FET

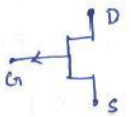
* Small gain bandwidth product.

Symbol :

n-channel



p-channel



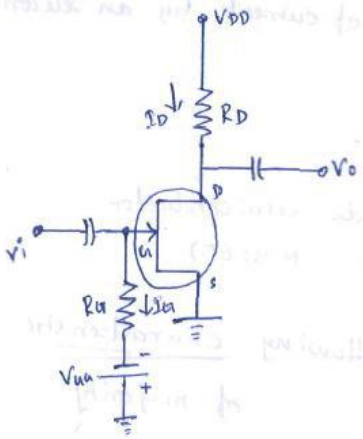
* The general relationship that can be applied to the dc analysis of all FET amplifiers are

$$I_G = 0 \text{ Amps}$$

$$I_D = I_S$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

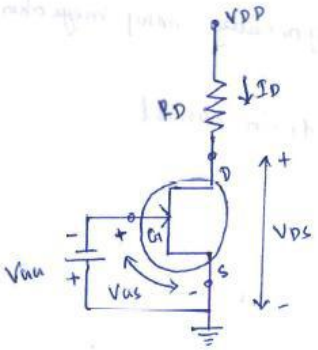
1. Fixed Bias / Gate Bias



* To make the Gate - source junction reverse biased a separate supply V_{GG} is connected such that gate is more negative than the source.

DC Analysis :

* For dc analysis coupling capacitors are open circuited.
* The current through R_G is I_G which is 0.
* This permits R_G to replace by short circuit equivalent, simplifying the fixed bias circuit.



* We know for dc analysis

$$I_G = 0 \text{ amps}$$

* Apply KVL to the Gate to source junction

$$V_{GS} + V_{GG} = 0$$

$$\therefore V_{GS} = -V_{GG}$$

* Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude & hence the name fixed bias circuit

* For fixed bias circuit the I_D can be calculated as

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

* Apply KVL to the Drain to Source junction

$$V_{DS} + I_D R_D - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D$$

Q-Point

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$V_{DSQ} = V_{DD} - I_{DQ} R_D$$