UNIT-IV VLSI TESTING

1. **What are the types of fault models?**
   - Stuck-at fault
   - Bridging fault
   - Stuck-open fault
2. **Define stuck-at fault?**

It is a faults in logic gates results in one of its inputs or output being fixed either

a logic 0 (stuck¬at-0) or a logic 1 (stuck-at-1).

3. **Define fault equivalence**

Two faults f and g are said to be functionally equivalent, iff $Z_f(x) = Z_g(x)$.

4. **Define sensitized path?**

A path composed of sensitized lines is called a sensitized path.

5. **State the lemma rule.**

Let G be the gate with inversion i and controlling value c, whose output is sensitized to a fault f(by a test t).

- All inputs of G sensitized to f have the same value (say a).
- All inputs of G not sensitized to f (if any have value c).
- The output of G has value a.

6. **What is redundancy?**

A combinational circuit that contains an undetectable struck fault is said to be redundant.

7. **Define fault dominance.**

Let Tg be the set of all tests that detect a fault g. we say that a fault f dominates the fault g if f and g are functionally equivalent under To.

8. **Give the algorithm for one pass strategy.**

for every event (i,v,')pending at the current time t begin

v(i) = Vi'

for every j on the

```
    fanout list of i
    begin
update input values of j
Vi'=evaluate (j) if vi
    *Isvo then begin
    schedule (j, vo) for
    time t+d(j)
lsv(j
    vo
    )
    en
    d
end
```

9. What are the proper lies of Single (Rote) stuck-at Bob?

Only one line is faulty.The faulty line is permanently set to 0 or 1.The fault can be at an input or output of a gate Simple logical model is independent of technology details

It reduces the complexity of fault description Algorithms.

10. Define bridging faults and mention its types?

Shorts between two or more signal lines are called as bridging faults. It can be classified into three types.

Input bridging faults Feedback bridging faults

Not Feedback bridging faults

11. What is controllability and observability?

Controllability is an ability to apply test patterns to the inputs of a sub circuit via primary of the circuit.

Observability is an ability to observe Me response of a sub circuit via the primary output of the circuit.

12. Define Backtrace

The procedure for obtaining a primary input assignment given an initial objective.

It is known as Backtrace.

13. **Mention any two methods used M test generation for sequential circuits**
    - State table verification
    - Testing of sequential circuits as iterative combinational circuits
14. **Draw the hardware model for delay fault testing?**

Input latches-----combinational logic circuits output latches

15. **What Is mean by homing sequence?**

To design checking experiment it is necessary to blow the initial state of the network,

which is determined by distinguish or homing sequence.

16. **List out the three phases of checking experiment?**
    - Initialization phase
    - State identification phase
    - Transition verification phase
17. **List out the advantages of LSSD techniques.**

The correct operation of the logic network is independent of nc characteristics such as clock edge rise tine and fall time. News is combinational in name as far as test generation and testing is concerned.

18. **What are the classifications of test points?**

Test points are classified into two types

Control points (CP) - CPs are primary inputs to enhance controllability. Observation points (OP) - Ops are primary outputs to enhance observability.

19. **Define Initialization?**

It is a process of bringing a sequential circuit into a known state at some known time, such as when it is powered on or after an initialization sequence is applied.

20. **List out the types of generic scan based design?**

Full serial
integrated
can Isolated

serial scan

Non serial scan

21. **State the LSSD design rules?**

All internal storage elements must consist of polarity hold latches. Latches can be controlled by two or more non overlapping clocks. Clock primary inputs cannot feed the data inputs to latches, either directly or through combinational logic. They may only feed clock inputs ti latches or primary outputs.

22. **List out the uses of scan design?**

Flipflops and latches are more complex. Hence scan designs are expensive in terms of board or silicon area. Some designs are not easily realizable as scan designs. Test generation costs can be significantly reduced. This can also lead to higher fault coverage.

23. **List out the categories of test pattern generation approaches for BIST?**

Exhaustive/Pseudo

exhaustive testing

Pseudo random testing

Deterministic testing

24. **What are the methods to derive n input and m output combinational circuit?**

- Syndrome driver counter
- Constant weight counter
- Linear feedback shift register/ shift register(LFSR/SR)
- Linear feedback shift register/ EX-OR gates(LFSR/EX-OR)

25. **List out the BIST architectures?**

- BILBO
- STUMPS
- LOCST

26. **Mention the test algorithms for RAMs?**

- GALPAT
- WALKING 0s AND 1s
- March Test
- Checkboard test

27. **List the types of coupling faults exist in memories**?

Inversion coupling fault

Idem-potent fault OR State coupling fault

28. **Mention the advantages of transition counting?**

It is not necessary to store either the correct response sequence or the actualresponse sequence at any test point; only the transition counts are needed.

29. **What are the advantages of circular BIST?**

It provides high fault coverage. Low hardware overhead.

30. **List out the methods of pseudo exhaustive pattern generation?**

Syndrome driver counter
Constant weight counter
LFSR/SR

31. **What is the need for testing?**

- During fabrication process several types of defects may exists such as catastrophic, crystalline.
- Catastrophic defect is due to contamination, resulting in destruction of all the transistors on the chip. And crystalline defect is because of destruction of a single transistor on the chip.
- It is necessary to the chip from the flaws. Hence it is mandatory to check the chip regarding its performance and functionality. Identifying the faulty chips creates huge difficulty in system debugging. It is also increase the debugging cost. Therefore the design for testability (DFT) is necessary.