SNS COLLEGE OF TECHNOLOGY

Coimbatore-35

An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++'(III Cycle) Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

23ECB201- DIGITAL SYSTEM DESIGN

II YEAR/ III SEMESTER

UNIT 1 – BOOLEAN THEOREMS AND LOGIC REDUCTION

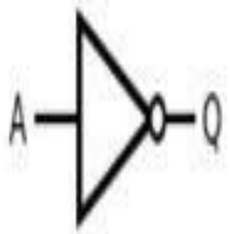
Topic – Implementation Using Universal Gates

NAND and NOR implementation

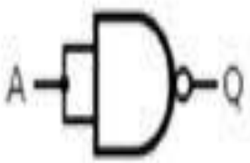
- Any Boolean function can be created using AND OR and NOT gates.
- AND, OR and NOT gates can be implemented using NAND and NOR gates.

NAND implementation - Implementation of NOT and AND using NAND gate

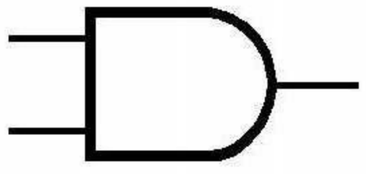
- A NAND gate with single input acts like a NOT gate.
- As a NAND gate is the invert of AND so by putting an inverter on the output of NAND we can have AND gate.



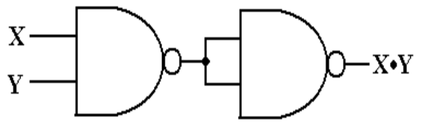
NOT gate



NAND construction of NOT gate

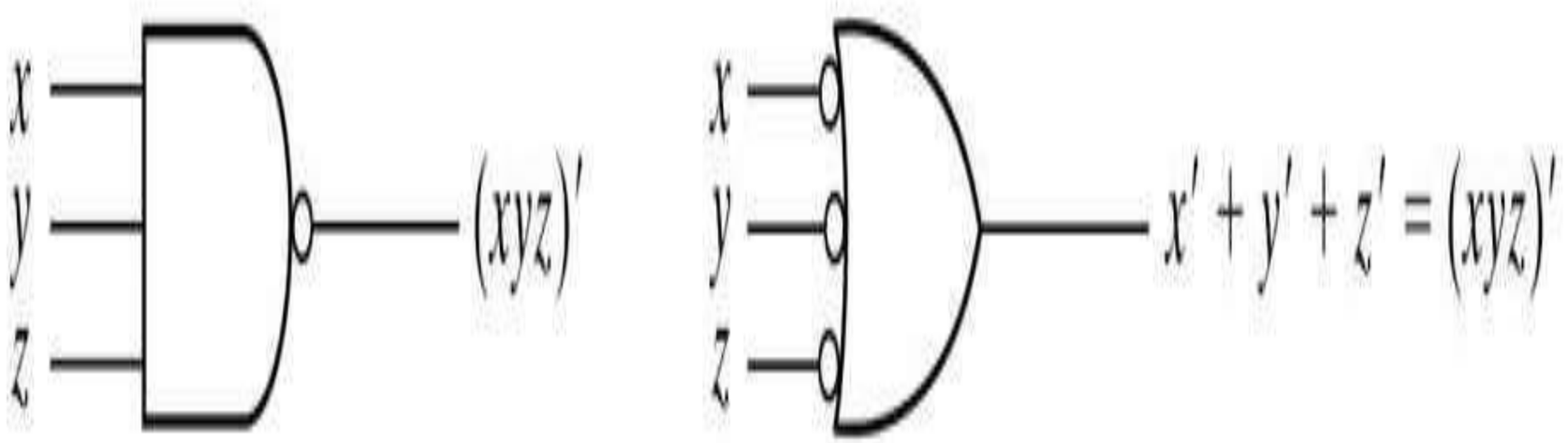


AND Gate



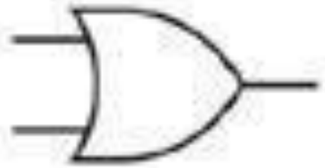
NAND Construction of ANDG ate

Symbolic Equivalence of NAND Gate

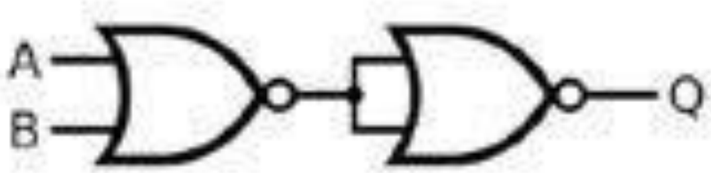


NOR implementation - Implementation of OR gate using NOR gate

- As NOR is the invert of OR gate so by putting an inverter in the output of NOR we get OR gate



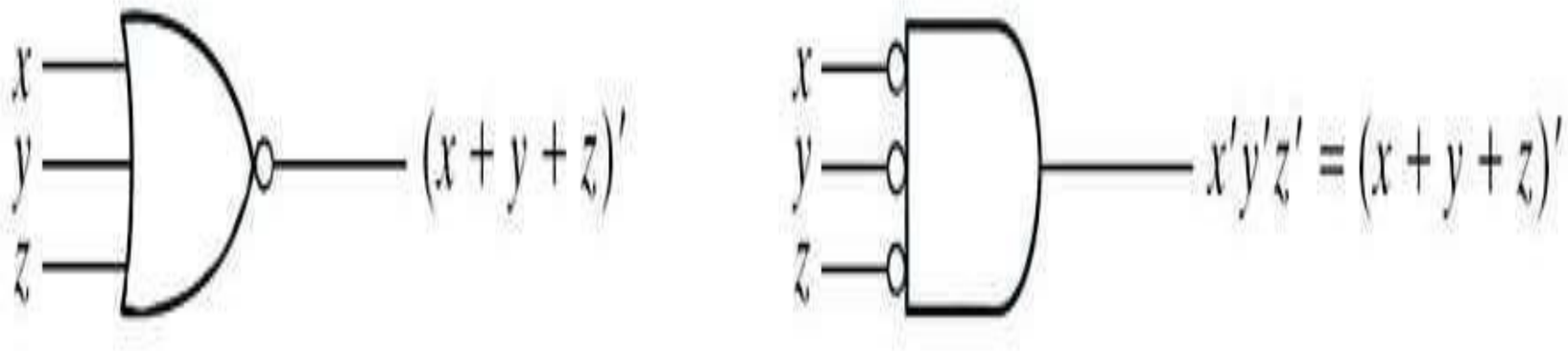
OR gate



NOR implementation of OR gate

Graphical equivalence of NOR gate

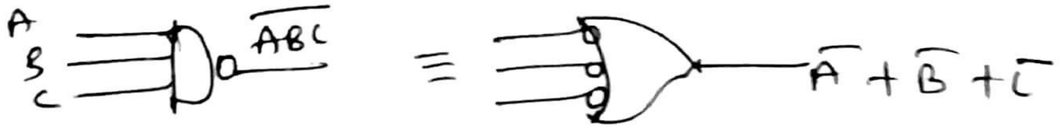
➢By De Morgan's Law we can describe NOR gate graphically by the following symbols



NAND – NOR Implementation :-

NAND – NAND Implementation :-

NAND = Bubbled OR (According to DE morgan's theorem)



Procedure :-

(i) Simplify the given logical expression and convert it in the SOP form.

(ii) Draw the AND – OR – NOT realization

(iii) Replace every AND gate by a NAND, every OR gate by a bubbled OR gate & NOT gate by a NAND inverter

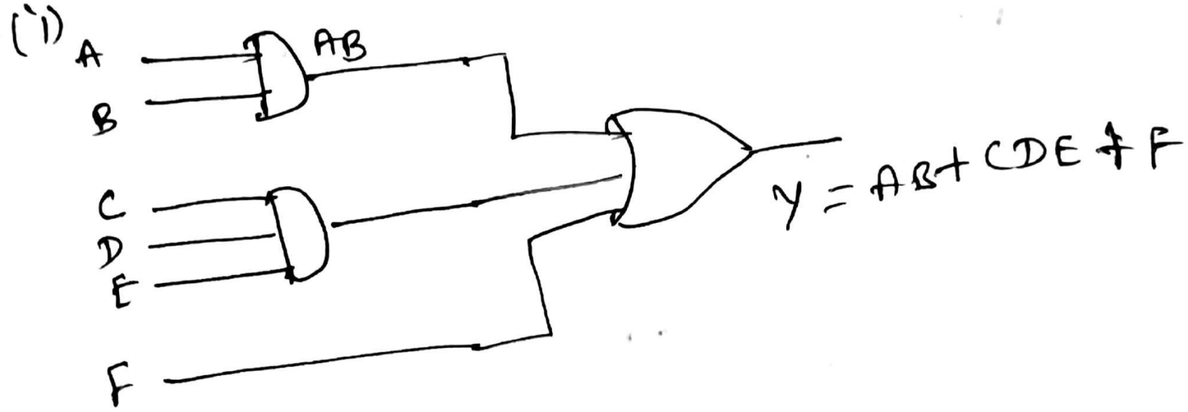
(iv) Finally draw the circuit using only NAND gates

Example

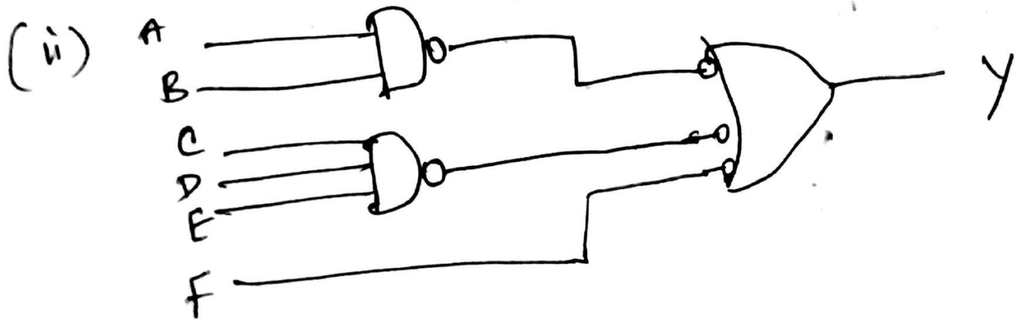
Implement the following Boolean function using only NAND gates.

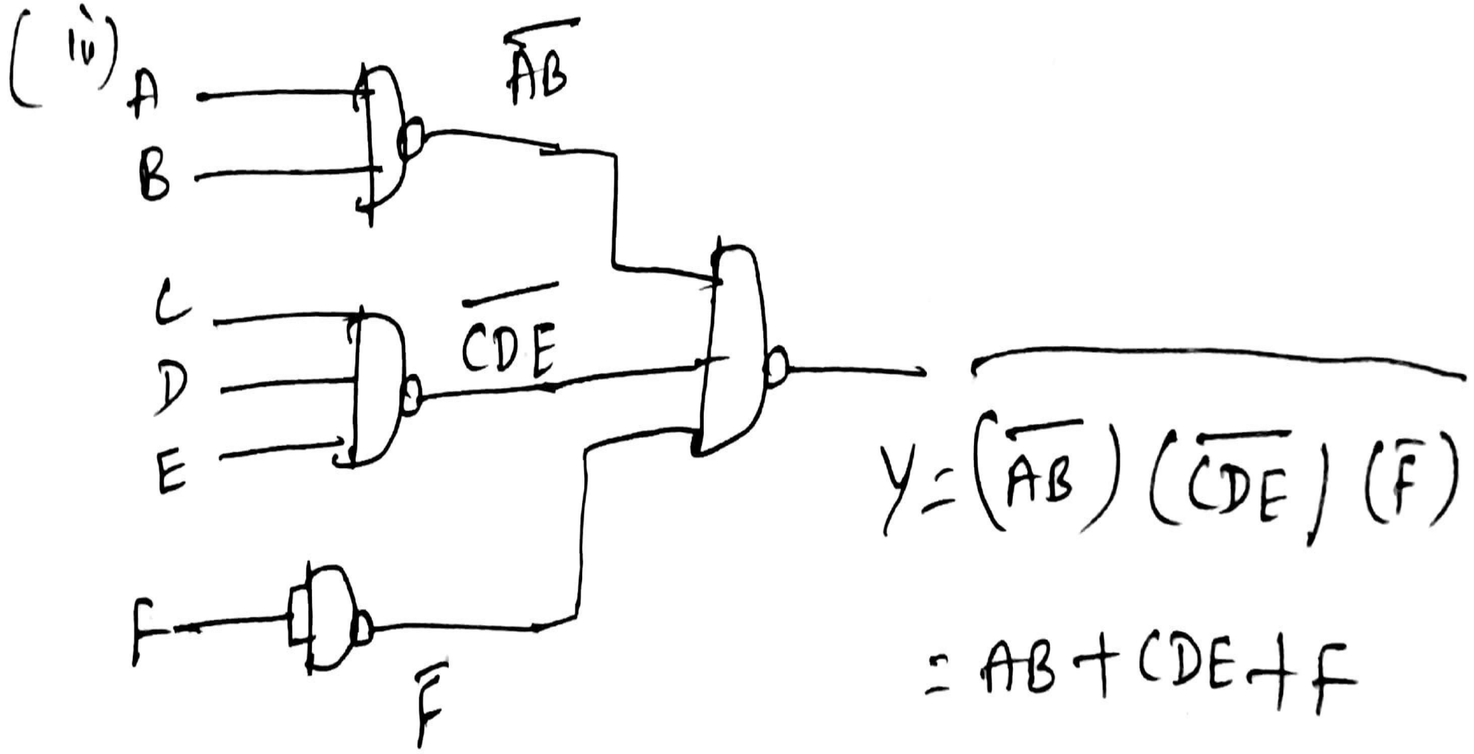
$$Y = AB + CDE + F$$

(i)



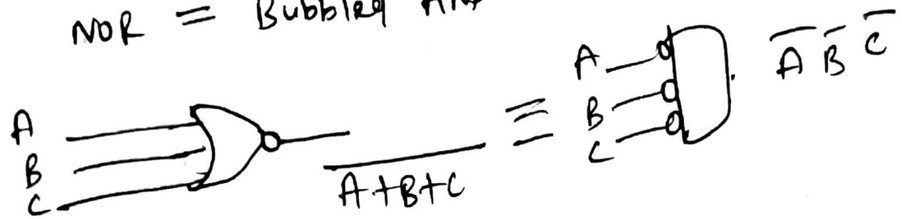
(ii)




(iv)
A
B
C
D
E
F
$\overline{AB}$
$\overline{CDE}$
$\overline{F}$
$Y = \overline{(\overline{AB})(\overline{CDE})(\overline{F})}$
$= AB + CDE + F$

NOR - NOR Implementation :-

NOR = Bubbled AND



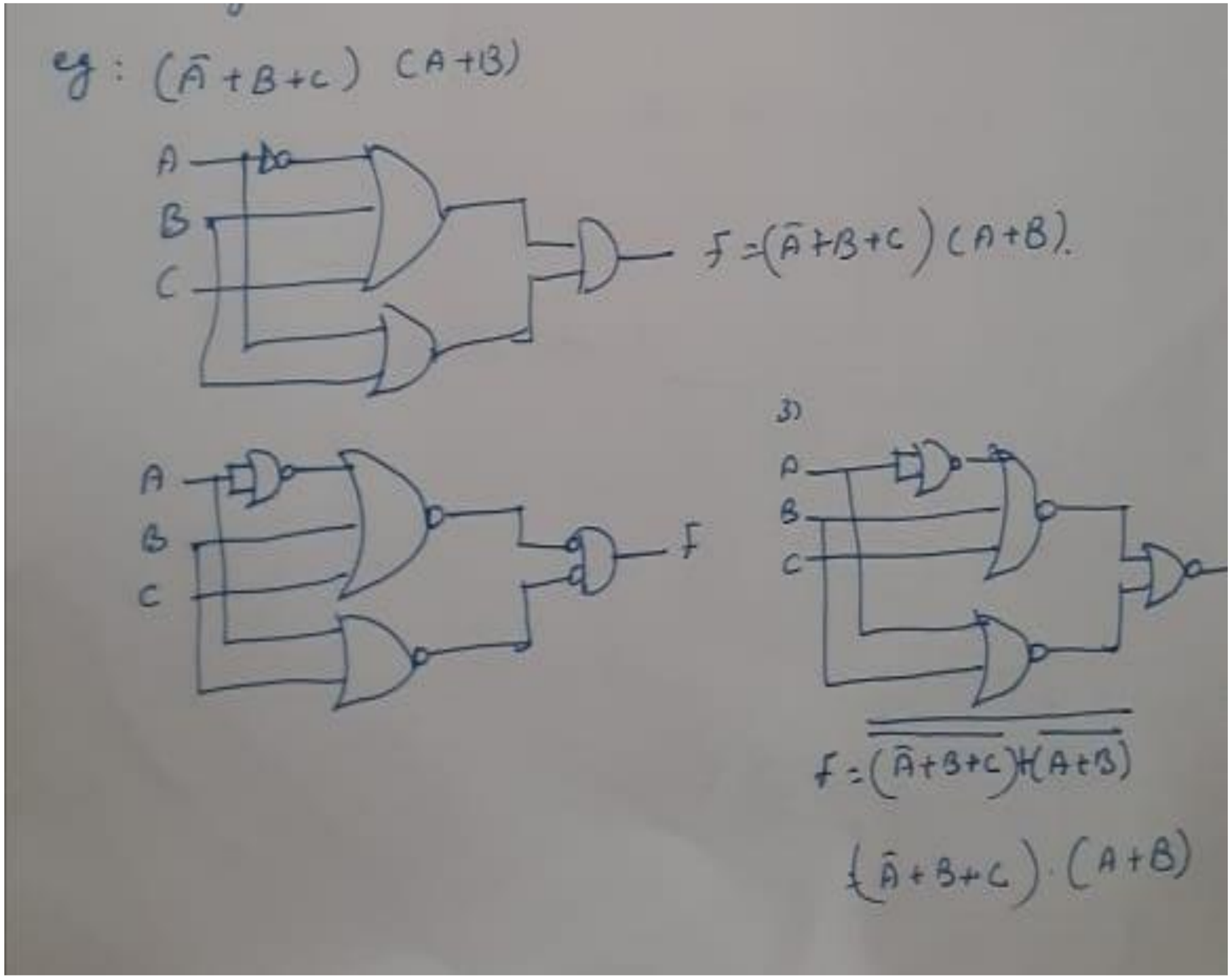
Procedure

(i) Expression convert it into POS form.

(ii) draw AND-OR-NOT realization

(iii) Replace every OR gate by NOR, AND by a bubbled AND gate and inverter by a NOR inverter

(iv) finally, draw the final circuit by only the NOR gates.


eg: $(\bar{A}+B+C)(A+B)$
A
B
C
$F=(\bar{A}+B+C)(A+B)$.
A
B
C
F
3)
A
B
C
$\overline{F=(\bar{A}+B+C)\overline{(A+B)}}$
$(\bar{A}+B+C)\cdot(A+B)$

THANK YOU