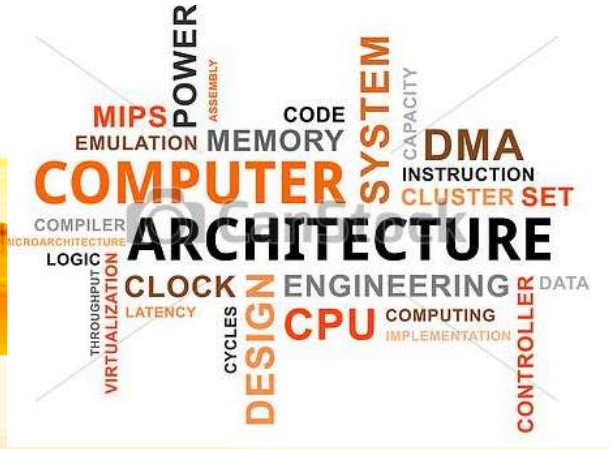
UNIT III
PROCESSOR AND PIPELINING

Fundamental concepts – Execution of a complete instruction – Multiple bus organization – Hardwired control – Micro programmed control – Pipelining: Basic concepts – Data hazards – Instruction hazards – **Influence on Instruction sets** – Data path and control consideration.



Recap the previous Class

HAZARDS

DATA HAZARDS

Need to wait for previous instruction

STRUCTURAL HAZARDS

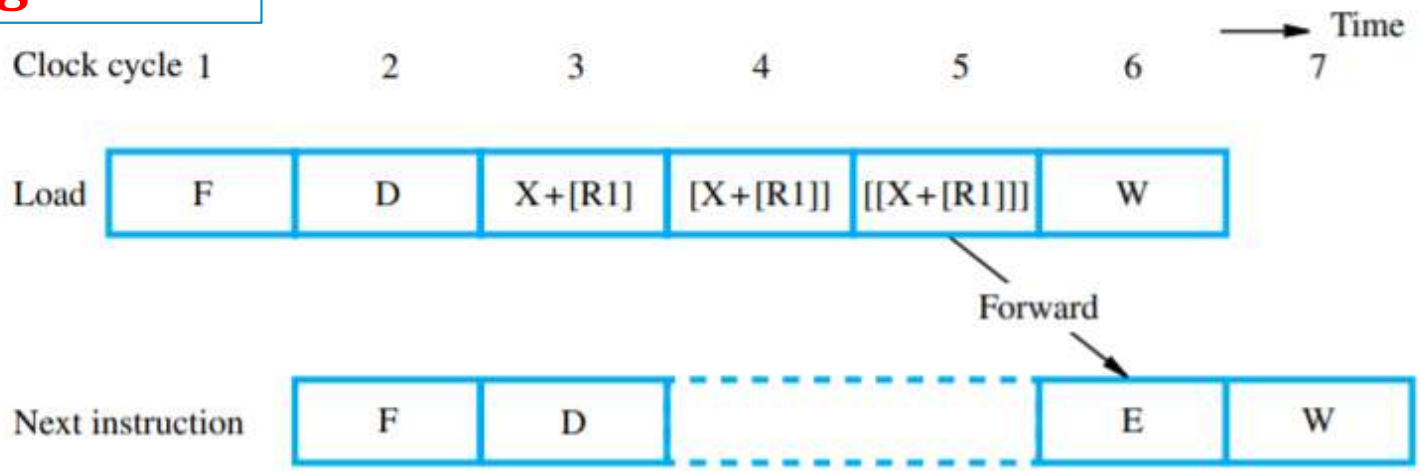
required resource is busy

CONTROL HAZARDS

Deciding on control action

Influence on instruction sets

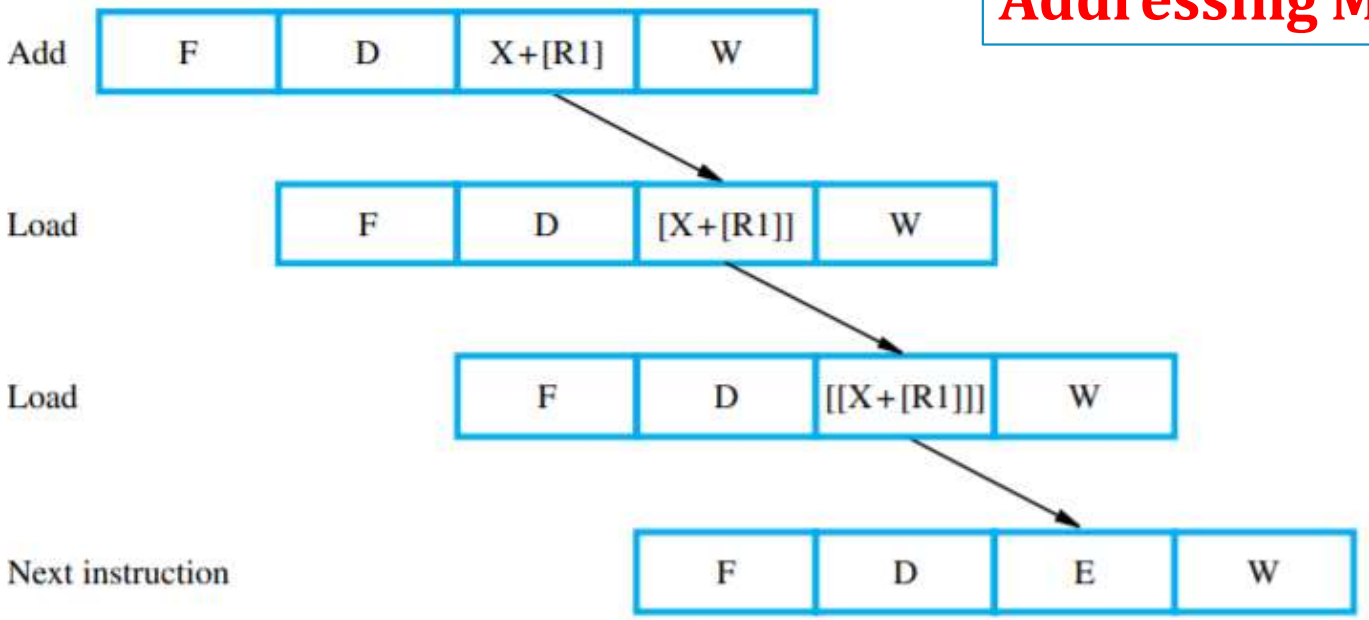
Addressing Modes



(a) Complex addressing mode

Influence on instruction sets

Addressing Modes



(b) Simple addressing mode

Influence on instruction sets

Conditional Flag

Instruction Reordering

Add	R1,R2
Compare	R3,R4
Branch=0	. . .

(a) A program fragment

Compare	R3,R4
Add	R1,R2
Branch=0	. . .

(b) Instructions reordered


Thank You