SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)

COIMBATORE-35

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23EET202 / DIGITAL ELECTRONICS AND LINEAR INTEGRATED CIRCUITS

II YEAR / III SEMESTER

UNIT-III: DESIGN OF SEQUENTIAL CIRCUITS, PLD, VHDL

DESIGN OF SEQUENTIAL CIRCUITS

TOPIC OUTLINE

Sequential Circuits – Counters

Design Procedure

Example – 2/3/4 bit counter

Recap

SEQUENTIAL CIRCUITS: COUNTERS

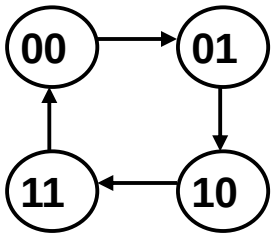
- **Counters** are circuits that cycle through a specified number of states.
- Two types of counters:
  - ❖ synchronous (parallel) counters
  - ❖ asynchronous (ripple) counters
- Ripple counters allow some flip-flop outputs to be used as a source of clock for other flip-flops.
- Parallel counters apply the same clock to all flip-flops.

DESIGN - PROCEDURE

- Read the problem statement given. Draw the state diagram according to it
- Develop a state table if required
- Develop excitation table with the question asked flip flop (if not choose 'T' flip flop)
- Derive the minimized expression using K map (note: use present state as input to the flip flop)
- Realize with logic gates and flip flops
- Practically implement this circuit using Logic ICs and verify the result

Synchronous (Parallel) Counters

- Synchronous (parallel) counters: the flip-flops are clocked at the same time by a common clock pulse.
- We can design these counters using the sequential logic design procedure.
- **Example 1 :** Design a 2-bit synchronous binary counter (using T flip-flops, or JK flip-flops with identical J,K inputs).



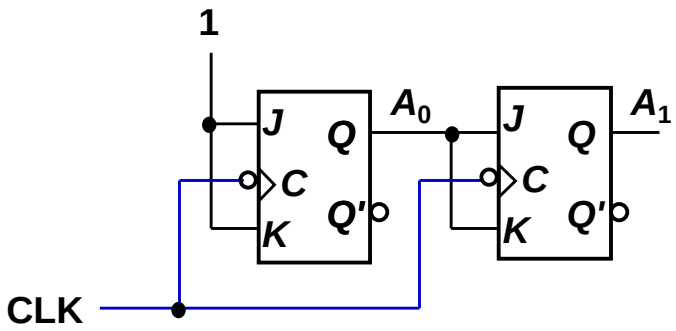
Present state		Next state		Flip-flop inputs	
A_1	A_0	A_1^+	A_0^+	TA_1	TA_0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

- 2-bit synchronous binary counter (using T flip-flops, or JK flip-flops with identical J,K inputs).

Present state		Next state		Flip-flop inputs	
A_1	A_0	A_1^+	A_0^+	TA_1	TA_0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

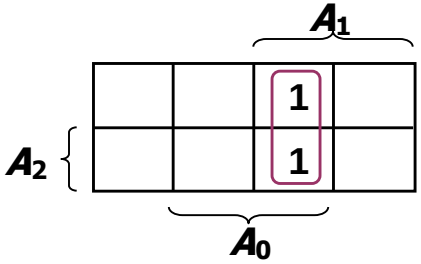
$TA_1 = A_0$

$TA_0 = 1$

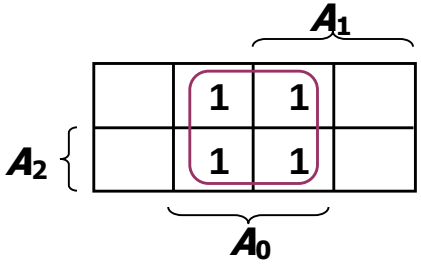


- **Example 2:** Design a 3-bit synchronous binary counter (using T flip-flops, or JK flip-flops with identical J, K inputs).

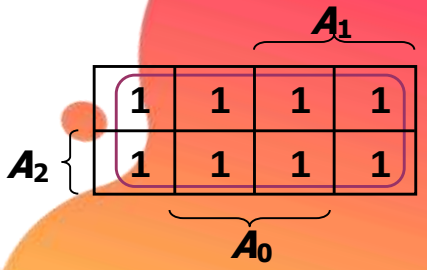
Present state			Next state			Flip-flop inputs		
A_2	A_1	A_0	A_2^+	A_1^+	A_0^+	TA_2	TA_1	TA_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1



$TA_2 = A_1.A_0$



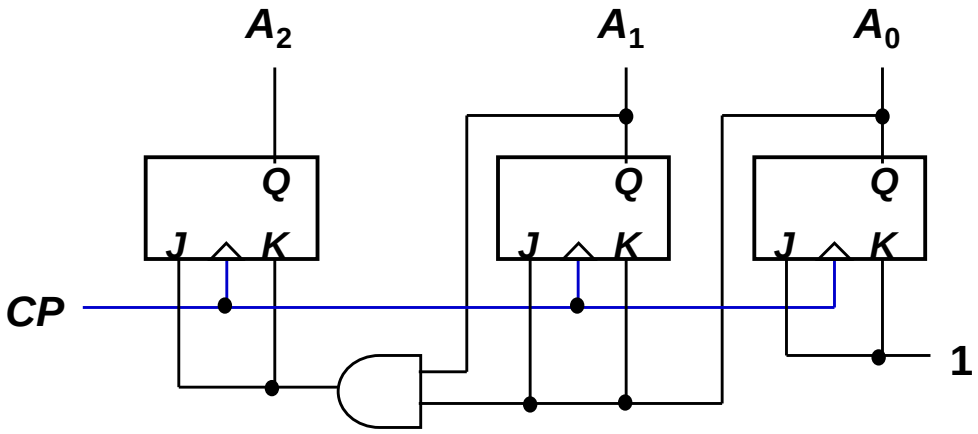
$TA_1 = A_0$



$TA_0 = 1$

- 3-bit synchronous binary counter (cont'd).

$TA_2 = A_1.A_0$ $TA_1 = A_0$ $TA_0 = 1$



- Note that in a binary counter, the n^{th} bit (shown underlined) is always complemented whenever

$$\underline{0}11\ldots11 \rightarrow \underline{1}00\ldots00$$

or $$\underline{1}11\ldots11 \rightarrow \underline{0}00\ldots00$$

- Hence, X_n is complemented whenever

$$X_{n-1}X_{n-2} \ldots X_1X_0 = 11\ldots11.$$

- As a result, if T flip-flops are used, then

$$TX_n = X_{n-1} \cdot X_{n-2} \cdot \ldots \cdot X_1 \cdot X_0$$

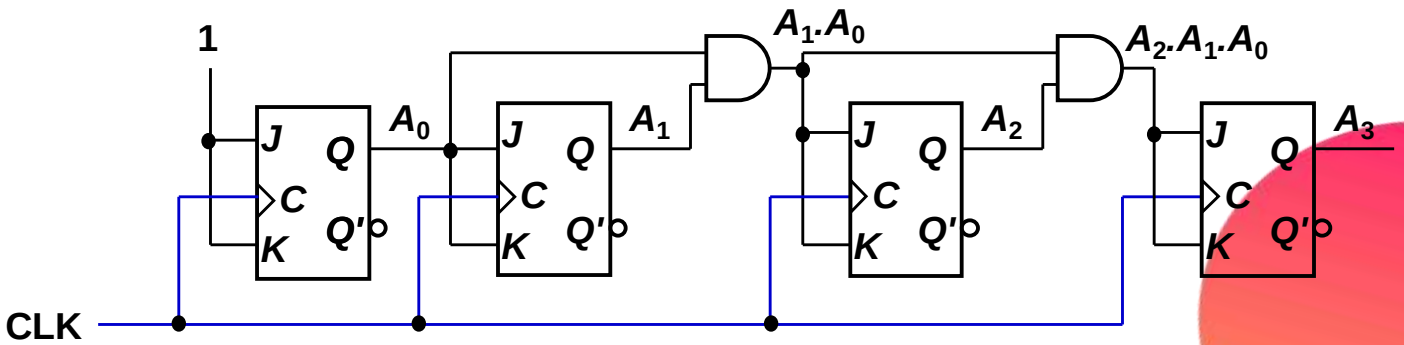
- **Example 3:** Design a 4-bit synchronous binary counter.

$TA_3 = A_2 \cdot A_1 \cdot A_0$

$TA_2 = A_1 \cdot A_0$

$TA_1 = A_0$

$TA_0 = 1$



RECAP..

Thank You